10 bit ADC with Serial Control

PRODUCT DESCRIPTION

The MS1549 is a 10bit, switched-capacitor and SAR analog-to-digital converter. It has two digital input terminals and one tri-state output terminal ($\overline{\text{CS}}$, I/O CLOCK and DATA OUT) which can complete the data transmission from three-wire interface to the serial interface of total controller.

The MS1549 has automatic sample-and-hold, proportional scale calibrating conversion range, anti-noise-interference functions. Switched-capacitor design makes the total error is only ±1 LSB (4.8mV) at full-scale. Therefore, the MS1549 can be widely used in the analog-to-digital conversion circuit.

SOP8

FEATURES

- 10bit ADC
- Internal Sample-and-Hold Function
- Total Unadjusted Error±1LSB (Max)
- On-chip System Clock
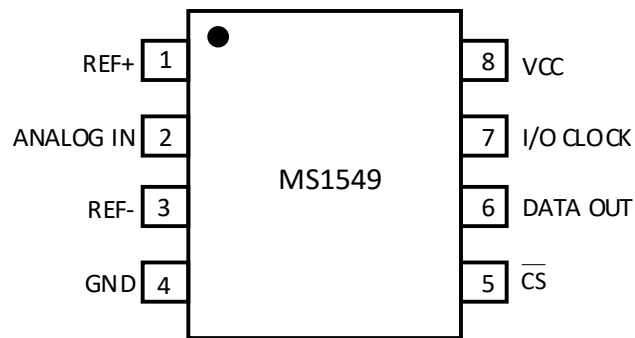- Pin Compatible with TLC549 and TLV1549
- COMS Technology

APPLICATIONS

- Analog-to-Digital Conversion like Senor

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS1549	SOP8	MS1549

PIN CONFIGURATION

```
           ┌─────────────────┐
    REF+  1│ ●               │8  VCC
          │                 │
ANALOG IN 2│                 │7  I/O CLOCK
          │    MS1549       │
    REF-  3│                 │6  DATA OUT
          │                 │
     GND  4│                 │5  CS̄
           └─────────────────┘
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PIN DESCRIPTION

Pin	Name	Typ	Description
1	REF+	I	The positive reference voltage (usually VCC) is connected to REF+ pin. The maximum input voltage range is the differential value of REF+ and REF- voltage.
2	ANALOG IN	I	Analog Signal Input. Power impedance should be less than 1kΩ. The current from external power to this pin should be more than 10mA.
3	REF-	I	The negative reference voltage (usually ground) is connected to REF- pin.
4	GND	-	The pin is connected with the ground of internal circuit. Unless otherwise noted, all ground are connected with this pin.
5	$\overline{CS}$	I	Chip Select. $\overline{CS}$ going high-level to low-level can reset the internal counter and it can control and enable DATA OUT, I/O CLOCK within a maximum startup time plus two fall times of internal clock. In addition, during the time period, $\overline{CS}$ going low-level to high-level can disable I/O CLOCK.
6	DATA OUT	O	When $\overline{CS}$ is high, AD conversion result is high-impedance. When $\overline{CS}$ is low, AD conversion result is valid. Under valid $\overline{CS}$, the output value on this pin is the digital value for the MSB of last conversion result. On the falling edge of next clock, the next most significant bit is output. According to the sequence until the LSB is output on the ninth falling edge. On the tenth falling edge, this pin is pulled low to ensure the transmission of serial data terminal is more than 10 clock periods.

Pin	Name	Typ	Description
7	I/O CLOCK	IO	Input/Output Clock Terminal. This pin acts as serial clock input, having following functions: (1) On the third clock falling edge, analog input voltage starts charging array capacitor until the tenth falling edge. (2) Along with this pin, remaining 9 bits of previous conversion result is output bit-by-bit on DATA OUT pin. (3) On the tenth falling edge, this pin can control conversion result to transmit to internal controller.
8	VCC	-	Positive Power Supply

BLOCK DIAGRAM
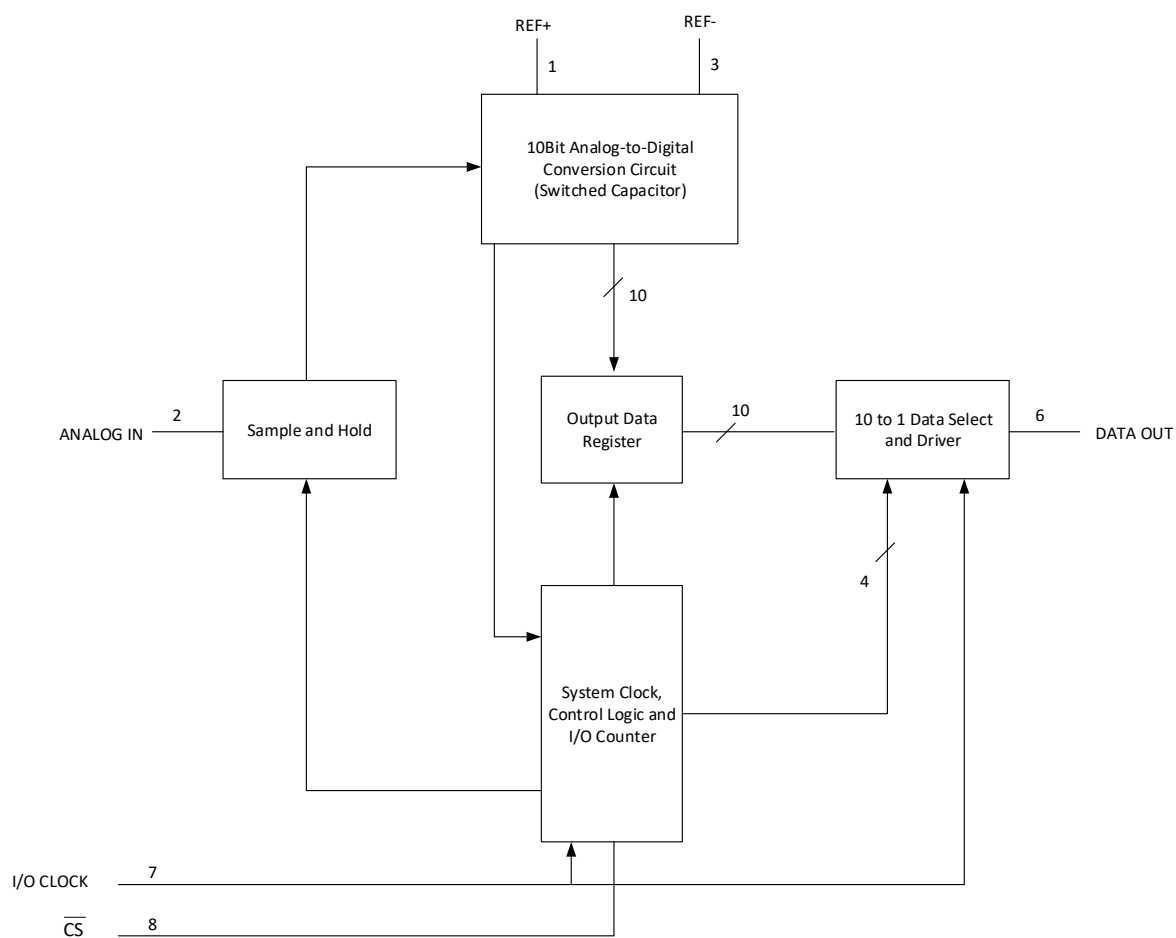
ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Range	Unit
Power Supply	-0.5 ~ 6.5	V
Input Range	-0.3V~ VCC+0.3	V
Output Range	-0.3 ~ VCC+0.3	V
Positive Reference Voltage	VCC+0.1	V
Negative Reference Voltage	-0.1	V
Input Peak Current	±20	mA
Total Peak Current	±30	mA
Vacuum Operating Temperature	0 ~ 70	°C
Storage Temperature	-65 ~ 150	°C

ELECTRICAL CHARACTERISTICS

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	VCC	2.7	5	5.5	V
Positive Reference Voltage	Vref+		VCC		V
Negative Reference Voltage	Vref-		0		V
Differential Reference Voltage	Vref+ - Vref-	2.5	VCC	VCC+0.2	V
Analog Input Voltage		0		VCC	V
Control Voltage High-level (VCC＝2.7V to 5.5V)		2			V
Control Voltage Low-level (VCC＝2.7V to 5.5V)				0.8	V
I/O CLOCK Frequency		0		2.1	MHz
Setup Time, $\overline{CS}$ Falling Edge to I/O CLOCK Rising Edge	tsu (CS)	1.425			μs
Hold Time, $\overline{CS}$ Rising Edge to I/O CLOCK Falling Edge	th (CS)	0			ns
I/O CLOCK High-level Time	twH (I/O)	190			ns
I/O CLOCK Low-level Time	twL (I/O)	190			ns
I/O CLOCK Level Transition Time	tt (I/O)			1	μs
$\overline{CS}$ Transition Time	tt (CS)			10	μs
Vacuum Operating Temperature			0	70	°C

Electrical Characteristics in Recommended Operating Conditions

VCC＝Vref+＝2.7V to 5.5V, I/O CLOCK frequency 2.1MHz.

All typical values are measured at VCC=5V, TA=25°C.

Parameter	Condition	Min	Typ	Max	Unit
VOH Output High-level	VCC=2.7V. IOH=-1.6mA	2.4			V
	VCC=2.7V~5.5V.IOH=-20μA	VCC-0.1			
VOL Output Low-level	VCC=2.7V, IOL=-1.6mA			0.4	V
	VCC=2.7V~5.5V, IOH=20μA			0.1	
IOZ High-impedance Output Current	Vo=VCC, $\overline{CS}$ at VCC			10	μA
	Vo=0, $\overline{CS}$ at VCC			-10	
IIH High-level Input Current	VI=VCC		0.005	2.5	μA
IIL Low-level Input Current	VI=0		-0.005	-2.5	μA
ICC Operating Current	$\overline{CS}$ =0		0.8	2.5	mA
Analog Input Leakage Current	VI=VCC			1	μA
	VI=0			-1	μA
Input Vref+ Quiescent Current	Vref+=VCC, Vref-=0			10	μA
Ci Input Capacitance	In sample period		30	55	pF

Operating Parameters in Recommended Vacuum Conditions

| Parameter	Symbol	Condition	Min	Max	Unit
EL linearity Error (Note 2)				±1	LSB
EZS Zero-scale Error (Note 3)		See Note 1		±1	LSB
EFS Full-scale Error (Note 3)		See Note 1		±1	LSB
Total Unadjusted Error (Note 4)				±1	LSB
Conversion Time	tconv			21	μs
Total Cycle Time (Sample, Hold and Convert)	tc			21+10 I/O CLOCK Period (Note 5)	μs
DATA OUT Valid Time after the I/O CLOCK Falling Edge	tv	See Figure Below	10		ns
Delay Time, I/O CLOCK Falling Edge to DATA OUT Valid	td	See Figure Below		240	ns
Enable Time, $\overline{CS}$ Falling Edge to DATA OUT	tPZH,tPZL	See Figure Below		1.3	μs
Disable Time, $\overline{CS}$ Rising Edge to DATA OUT	tPHZ,tPLZ	See Figure Below		180	ns
Rise Time for Data Bus	tr(bus)	See Figure Below		300	ns
Fall Time for Data Bus	tf(bus)	See Figure Below		300	ns
Delay Time, Tenth I/O CLOCK Falling Edge to $\overline{CS}$ Falling Edge (Note 6)	td (I/O-$\overline{CS}$)			9	μs

Note:

1. When analog input voltage is higher than REF+, conversion output is all 1. When analog input voltage is lower than REF-, conversion output is all 0. The input voltage range of the MS1549 can be low to 1V (Vref+ - Vref-). At this time, recommended electrical parameters are not applicable.

2. Linearity error is that the actual conversion output deviating from the best input/output characteristic straight line.

3. Zero-scale error is the difference between all 0 and the output for zero input voltage. Full-scale error is the difference between all 1 and the output for full-scale input voltage.

4. Total unadjusted error consists of linearity error, zero-scale error and full-scale error.

5. I/O CLOCK Period=1/(I/O CLOCK Frequency). Sample starts from the third I/O CLOCK falling edge and lasts seven I/O CLOCK periods and finishes on the tenth I/O CLOCK falling edge.

6. $\overline{CS}$ transition is only valid only when the level maintains for a minimum setup time plus two fall time of internal clock after the transition.
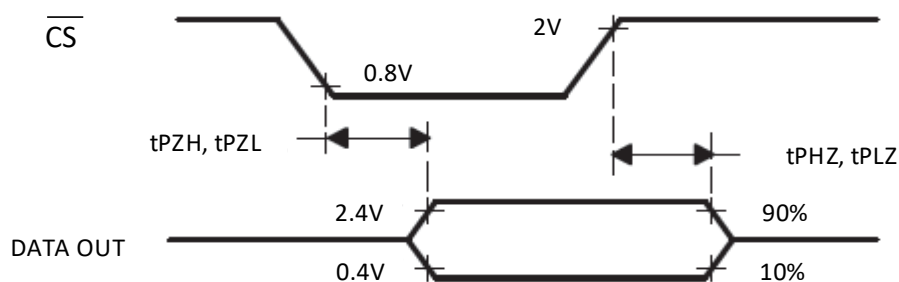
DATA OUT to Hi-Z Waveform
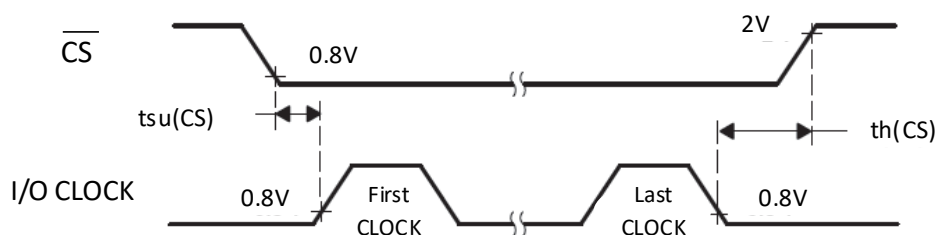
$\overline{CS}$ to I/O CLOCK Waveform
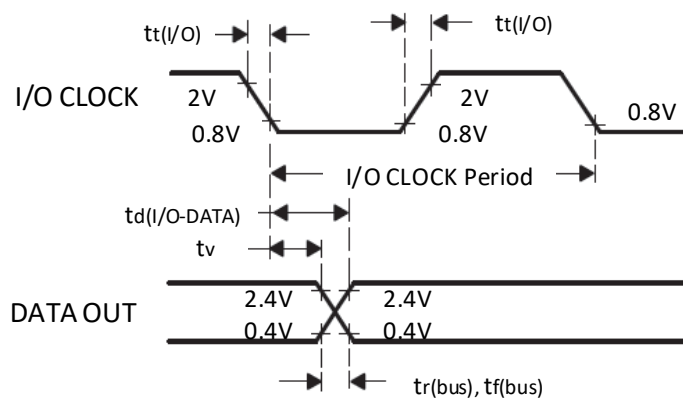
I/O CLOCK and DATA OUT Waveform

FUNCTION DESCRIPTION

When $\overline{CS}$ is high-level, I/O CLOCK is initially disabled and DATA OUT is high-impedance state. When the serial interface pulls $\overline{CS}$ low, the data conversion begins with enabling CLOCK and DATA OUT. The serial interface starts to provide one sequence clock and receive the previous conversion result on DATA OUT. Set 10 and 16 clocks periods for CLOCK by serial interface. Sampling the analog signal is completed within the first ten clocks periods.

The MS1549 has six basic serial interface time modes that depend on clock speed and $\overline{CS}$ operation. These modes include:

Mode 1: (Fast Mode) 10 clock periods for conversion time and $\overline{CS}$ high.

Mode 2: (Fast Mode) 10 clock periods for conversion time and $\overline{CS}$ low.

Mode 3: (Fast Mode) 11~16 clock periods for conversion time and $\overline{CS}$ high.

Mode 4: (Fast Mode) 16 clock periods for conversion time and $\overline{CS}$ low.

Mode 5: (Slow Mode) 11~16 clock periods for conversion time and $\overline{CS}$ high.

Mode 6: (Slow Mode) 16 clock periods for conversion time and $\overline{CS}$ low.

In the mode 1, 3, 5, after $\overline{CS}$ falling edge, DATA OUT pin starts to output the MSB of conversion.

In the mode 2 and 4, within 21μs after the tenth clock falling edge, DATA OUT starts to output the MSB of conversion.

In the mode 6, after the sixteenth clock falling edge, DATA OUT starts to output the MSB of conversion. In following nine clock falling edges, remaining 9bits are bit-by-bit output. The number of clock pulse is decided by selected operation mode. But for conversion startup, the minimum 10 clock pulses are needed. If more than 10 clock pulses, internal logic would pull DATA OUT low to ensure the remaining bits are cleared on the tenth clock falling edge.

All modes need a minimum 21μs delay time after the tenth clock falling edge before next conversion begins. During serial data transmission, $\overline{CS}$ must be low to ensure enabling I/O CLOCK. $\overline{CS}$ state is latched when data transmission in the modes 1, 3, and 5. $\overline{CS}$ transition is thank as valid only when the level maintains for at least 1.425μs after the transition. In the modes 3, 4, 5, and 6, If the transmission time is more than ten clock period, the eleventh clock rising edge must occur within 9.5μs after the tenth falling edge. Otherwise host serial interface may not synchronize. $\overline{CS}$ would toggle to recovery correct operation mode.

Fast Mode

In fast mode, serial clock transmission would be completed within 21μs after the tenth clock falling edge. In a 10-clock-period serial transmission, can only operate fast mode.

Mode 1: Fast mode, $\overline{CS}$ high between data transmission, 10-clock period.
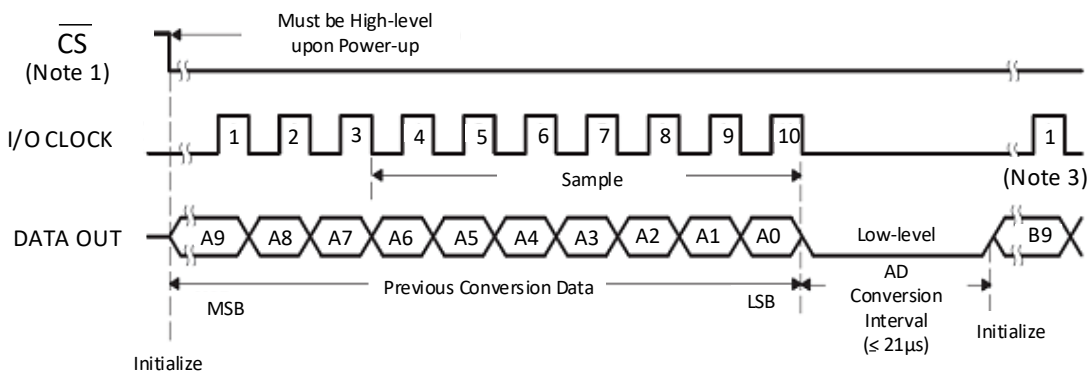
In this mode, each data transmission is ten-clock period and $\overline{CS}$ becomes high during this time. When the falling edge of $\overline{CS}$ starts, DATA OUT removes high-impedance state. When the rising edge of $\overline{CS}$ ends, DATA OUT returns to high-impedance state within the specified time. In addition, the rising edge of $\overline{CS}$ disables I/O CLOCK within a startup time plus two falling edges of the internal system clock. The timing is as follows:
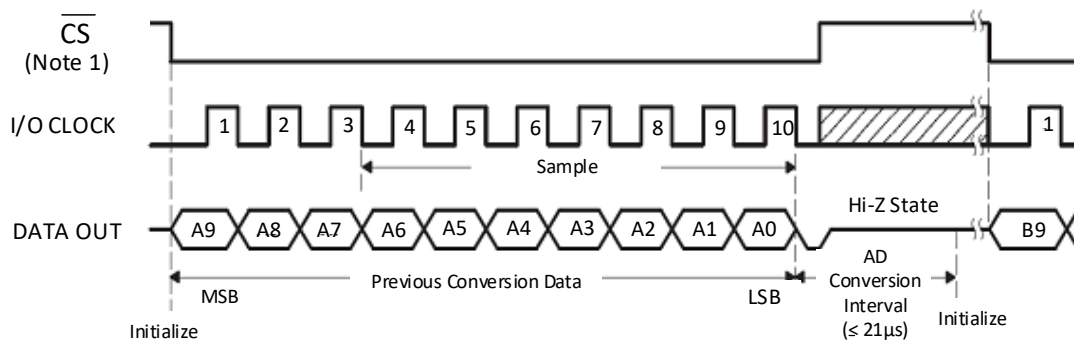
Mode 1 : 10-Clock Transmission Period with $\overline{CS}$ High

Mode 2: Fast mode, $\overline{CS}$ low between data transmission, 10-clock period.
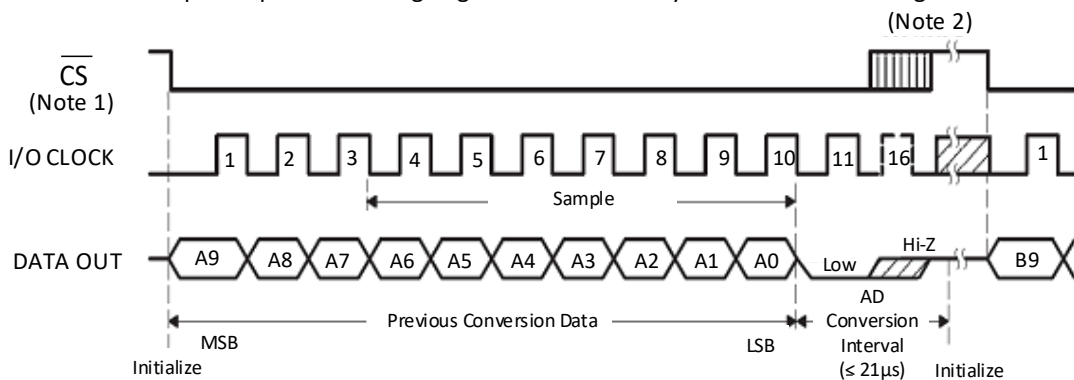
In this mode, each data transmission is ten-clock period and $\overline{CS}$ becomes low during this time. After initializing the conversion period, $\overline{CS}$ remains low-level for subsequent conversions. Within 21μs after the tenth falling edge, DATA OUT outputs the MSB of the previous conversion. The timing is as follows:

Mode 2 : 10-Clock Transmission Period with $\overline{CS}$ Low

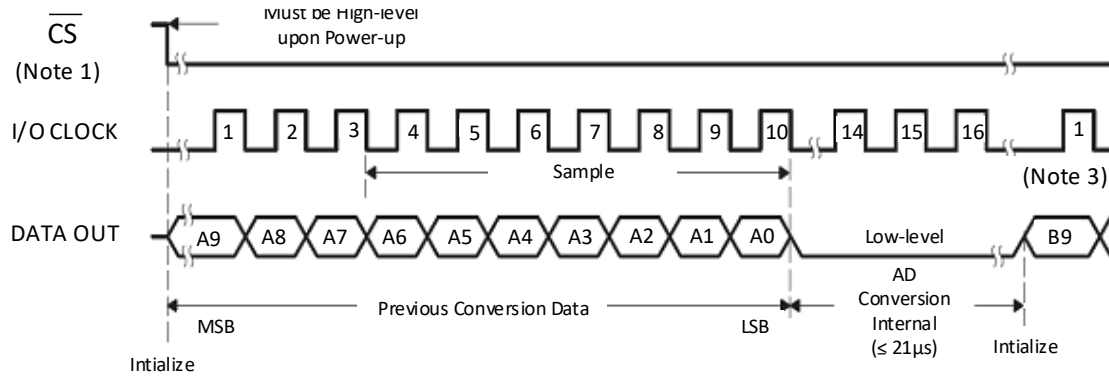Mode 3: Fast mode, $\overline{CS}$ high between data transmission, 11~16 clock period.

In this mode, each data transmission is 11 to 16 period and $\overline{CS}$ becomes high during this time. When the falling edge of $\overline{CS}$ starts, DATA OUT removes high-impedance state. When the rising edge of $\overline{CS}$ ends, DATA OUT returns to high-impedance state within the specified time. In addition, the rising edge of $\overline{CS}$ disables I/O CLOCK within a startup time plus two falling edges of the internal system clock. The timing is as follows:

Mode 3 : 11 to 16 Clock Transmission Period with $\overline{CS}$ High (Completed within 21μs)

Mode 4: Fast mode, $\overline{CS}$ low between data transmission, 16-clock period.

In this mode, each data transmission is sixteen-clock period and $\overline{CS}$ becomes low during this time. After initializing the conversion period, $\overline{CS}$ remains low-level for subsequent conversions. Within 21µs after the tenth falling edge, DATA OUT outputs the MSB of the previous conversion. The timing is as follows:
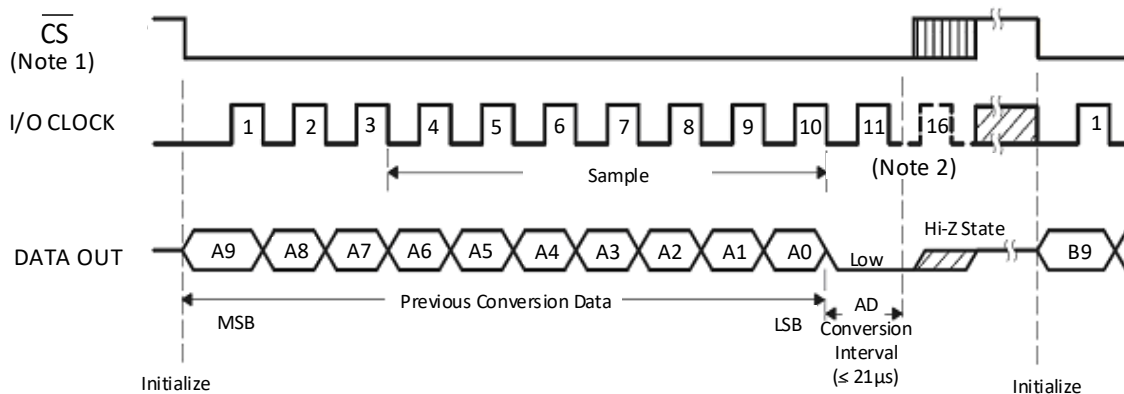

Mode 4 : 16-Clock Transmission Period with $\overline{CS}$ Low (Completed within 21µs)

Slow Mode

In slow mode, the serial clock data transmission is completed within 21µs after the tenth clock falling edge. Mode 5: Slow mode, $\overline{CS}$ high between data transmission, 11~16 clock period.

In this mode, each data transmission is 11 to 16 period and $\overline{CS}$ becomes high during this time. When the falling edge of $\overline{CS}$ starts, DATA OUT removes high-impedance state. When the rising edge of $\overline{CS}$ ends, DATA OUT returns to high-impedance state within the specified time. In addition, the rising edge of $\overline{CS}$ disables I/O CLOCK within a startup time plus two falling edges of the internal system clock. The timing is as follows:

Mode 5 : 11 to 16 Clock Transmission Period with $\overline{CS}$ High (Completed after 21µs)

Mode 6: Slow mode, $\overline{CS}$ low between data transmission, 16-clock period.

In this mode, each data transmission is sixteen-clock period and $\overline{CS}$ becomes low during this time. After initializing the conversion period, $\overline{CS}$ remains low-level for subsequent conversions. After the sixteen clock falling edges, DATA OUT removes low-level state and starts new conversion period, allowing DATA OUT pin to output the MSB of the previous conversion. Then the device is ready for the next 16-clock conversion initiated by the serial interface. The timing is as follows:
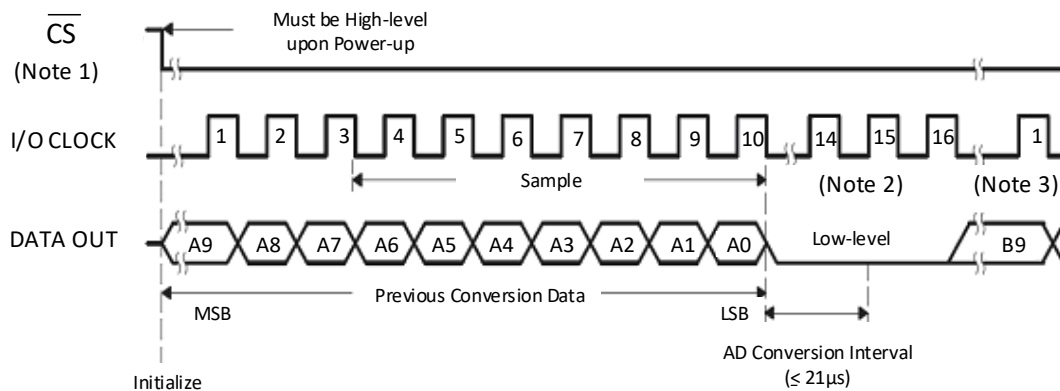
Mode 6 : 16-Clock Transmission Period with $\overline{CS}$ Low (Completed after 21μs)
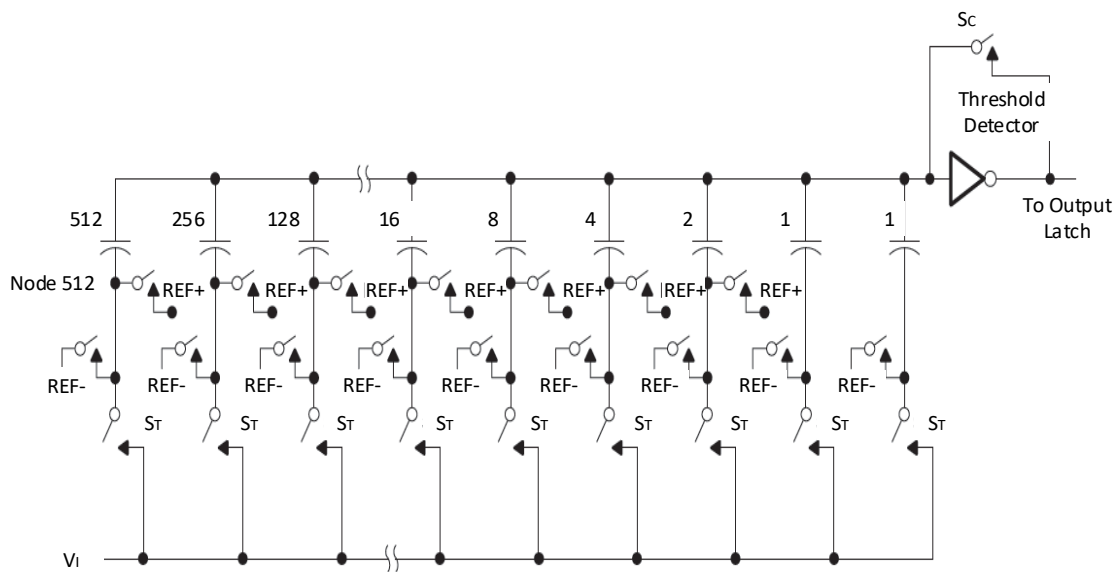
Note:

1. To reduce errors caused by $\overline{CS}$ noise, the internal circuit needs the wait time for a startup time plus two falling edges of the internal system clock after the falling edge of $\overline{CS}$. Then respond to I/O CLOCK. The data is output until the minimum $\overline{CS}$ setup time has elapsed.

2. The rising edge of $\overline{CS}$ disables I/O CLOCK within a startup time plus two falling edges of the internal system clock.

3. The first I/O CLOCK must occur at the end of the previous conversion.

Analog Input Sample

　Analog input sample starts after the third clock falling edge, and lasts for seven clock periods. The sample value is held on the tenth falling edge.

Converter and Analog Input

　The CMOS threshold detector determines each bit by detecting the charge voltage on a series of capacitors. In the first phase of the conversion process, the analog input is sampled by closing the SC and ST simultaneously. This process enables the charge voltage sum of all capacitors to reach the input voltage of ADC. In the second phase of the conversion process, all ST and SC are opened and threshold detector determines every bit by recognizing the charge voltage on each capacitor to approach the reference voltage. In this process, ten capacitors are detected one by one until ten bits are determined to convert. In the first step of the conversion phase, threshold detector detects the first capacitor (weight=512). Node 512 of this capacitor is switched to the REF+, and the same nodes of all the other capacitors are switched to REF-. If the voltage on the total node is more than the trip point of threshold detector (approximately half of VCC), bit 0 would be transmit to output register and node 512 is switched to REF-. If the voltage on the total node is less than the trip point of threshold detector, bit 1 would be transmit to output register and 512-weight capacitor still is connected to REF+ during the remaining successive approximation process. For 256-weight capacitor and 128-weight capacitor, the successive approximation process is repeated until all bits are determined from MSB to LSB.

Chip Select

$\overline{CS}$ transition can start all modes and stops any mode conversion. In specified time, when $\overline{CS}$ goes from high to level, the device would return to initial state (output register still remains the previous conversion result) . It is noted that if $\overline{CS}$ is pulled at the end of conversion, data may be lost.

Reference Input

The MS1549 has two reference voltages, REF+ and REF-. These two voltage values set the upper and lower limit of analog input voltage respectively. Analog input voltage cannot exceed power supply and cannot be less than GND. When input signal is more than or equal to REF+, digital output is full-scale. When input signal is less than or equal to REF-, digital output is 0.

Typical Application Diagram
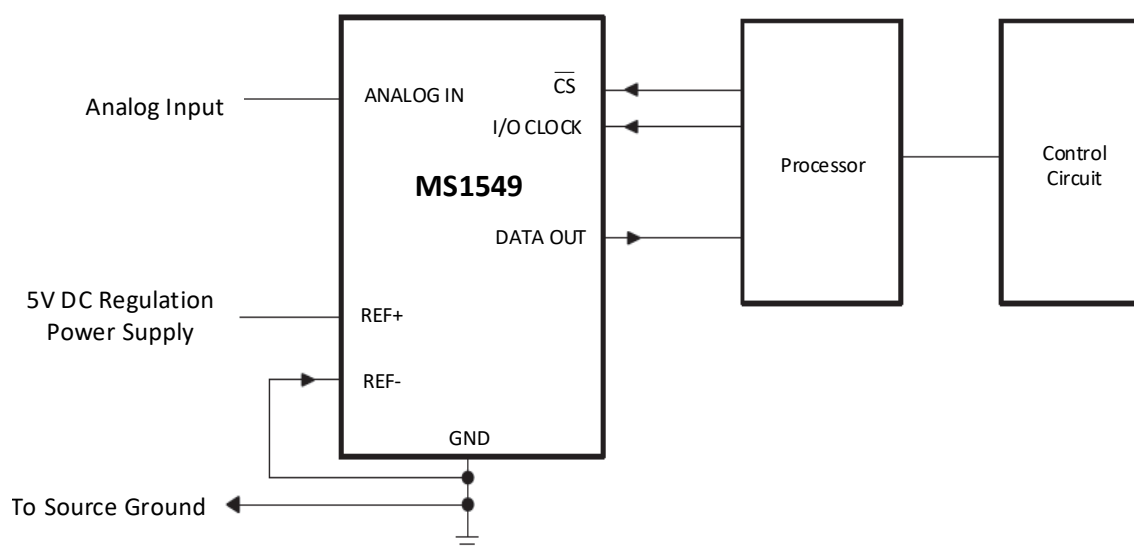
PACKAGE OUTLINE DIMENSIONS

SOP8
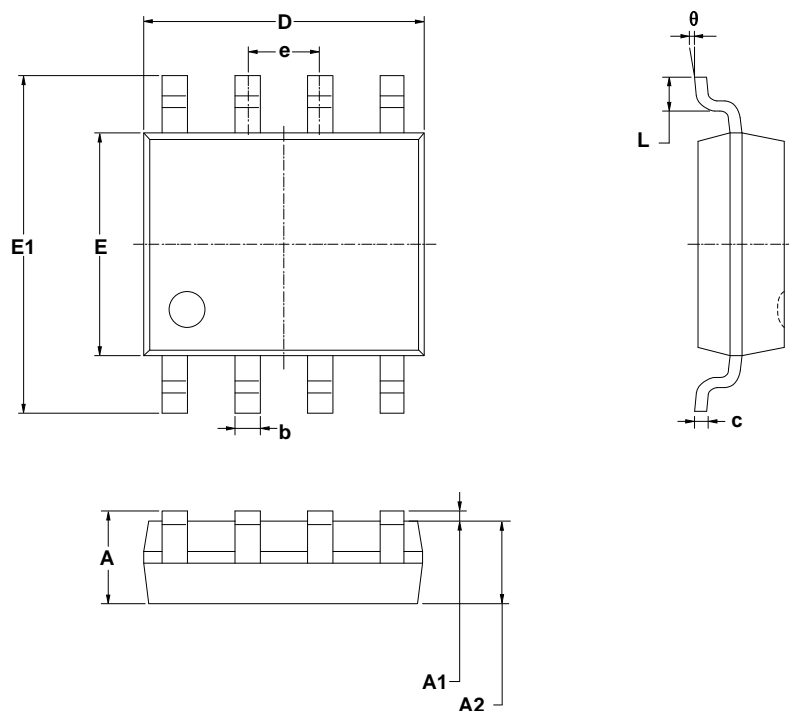
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0 º	8 º	0 º	8 º

MARKING and PACKAGE SPECIFICATIONS

1. Marking Drawing Description
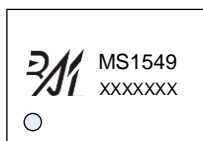
Product Name : MS1549

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS1549	SOP8	2500	1	2500	8	20000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

  Customer should get latest version information and verify the integrity before placing order.

- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety

  standard and adopt corresponding precautions, in order to avoid personal injury and property loss

  caused by potential failure risk.

- The process of improving product is endless. And our company would sincerely provide more excellent

  product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken

to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.

2. The equipment shell must be grounded.

3. The tools used in the assembly process must be grounded.

4. Must use conductor packaging or anti-static materials packaging or transportation.

+86-571-89966911

Rm701, No.9 Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

http:// www.relmon.com