24bit High Precision, Low Power Dissipation ADC

PRODUCT DESCRIPTION

The MS1242/MS1243 is a high-precision, wide dynamic range, Δ-Σ analog-to-digital converter with 24-bit no missing codes and 21-bit effective resolution. The MS1242/MS1243 can be applied widely in different fields like industrial control, weighing, liquid/gas chemical analysis, blood analysis, intelligent transmitter and portable measurement.

TSSOP16

TSSOP20

FEATURES

- 24 Bits No Missing Codes, 21 Bits Effective Resolution
- Integrated 50Hz and 60Hz Notch Filters
- INL: Less than 0.0015%
- Programmable Gains from 1 to 128
- Single-cycle Setup Time
- Programmable Data Output Rate
- External Reference Voltage: 0.1V to 5V
- Integrated Calibration Function
- Compatible with SPI
- Low Power Consumption
- Four Analog Input Channels (MS1242)
- Eight Analog Input Channels(MS1243)

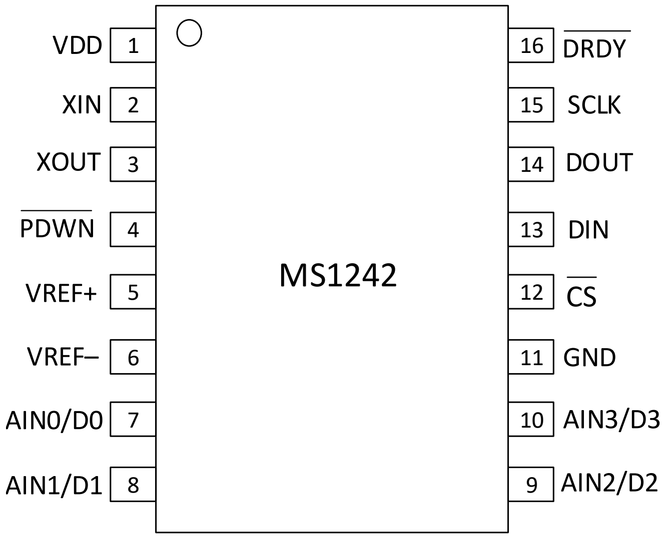
APPLICATIONS

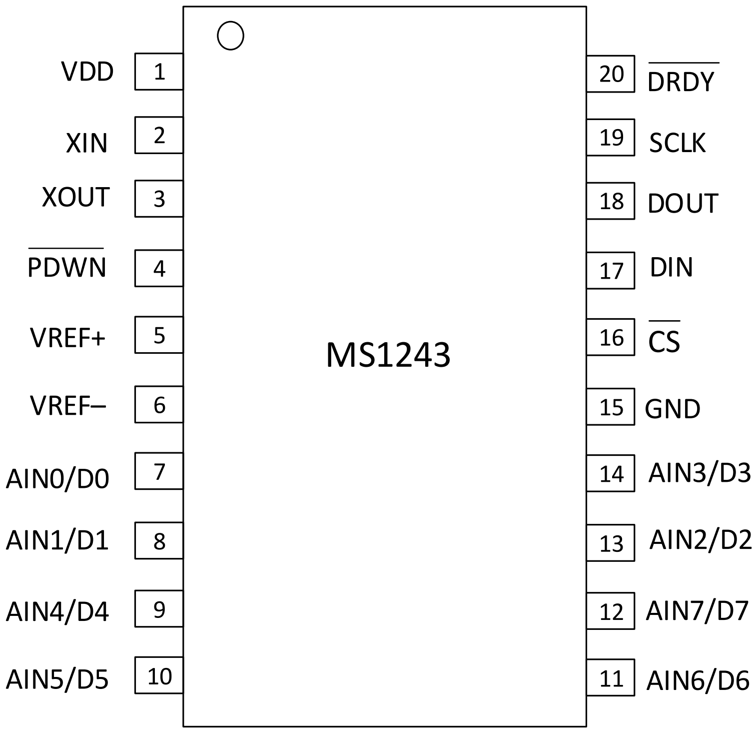
- Industrial Process Control
- Weight Scale
- Liquid/Gas Chemical Analysis
- Blood Analysis
- Intelligent Transmitters
- Portable Instrumentation

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS1242	TSSOP16	MS1242
MS1243	TSSOP20	MS1243

PIN CONFIGURATION





PIN DESCRIPTION

MS1242

Pin	Name	Type	Description
1	VDD	-	Power Supply
2	XIN	I	Clock Input
3	XOUT	O	Clock Output
4	$\overline{\text{PDWN}}$	I	Power-down Control Signal. Active Low
5	VREF+	I	Positive Reference Voltage Input
6	VREF–	I	Negative Reference Voltage Input
7	AIN0/D0	I	Analog Input 0/Data IO 0
8	AIN1/D1	I	Analog Input 1/Data IO 1
9	AIN2/D2	I	Analog Input 2/Data IO 2
10	AIN3/D3	I	Analog Input 3/Data IO 3
11	GND	-	Ground
12	$\overline{\text{CS}}$	I	Chip Select. Active Low
13	DIN	I	SPI Data Input
14	DOUT	O	SPI Data Output
15	SCLK	I	SPI Clock Input
16	$\overline{\text{DRDY}}$	O	Data Ready Indication Signal. Active Low

MS1243

Pin	Name	Type	Description
1	VDD	-	Power Supply
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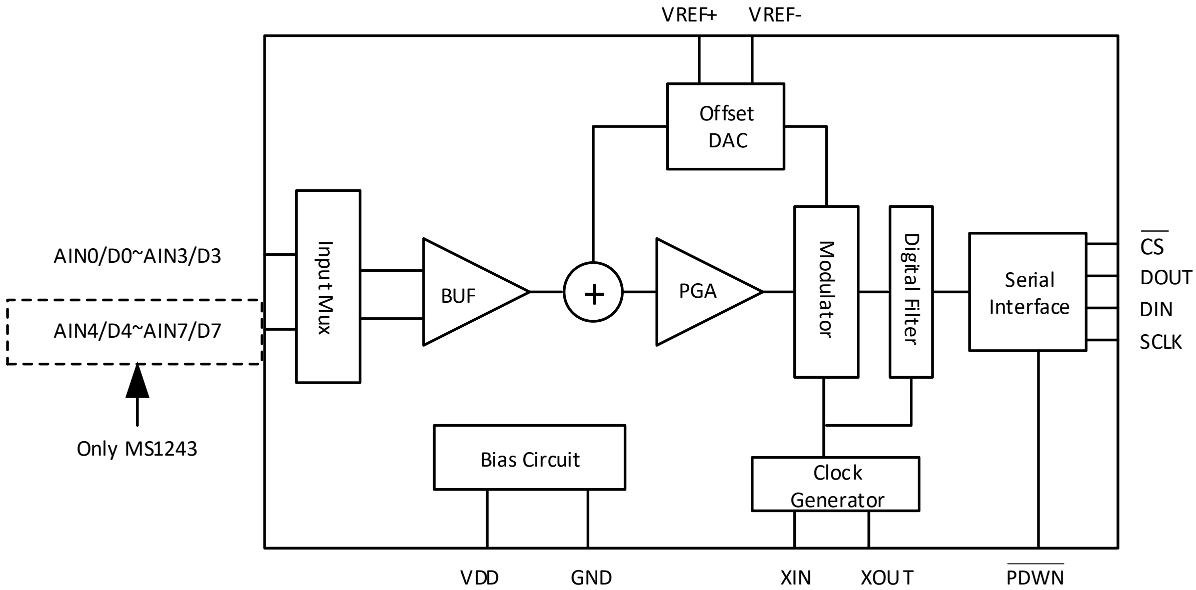
6	VREF–	I	Negative Reference Voltage Input
7	AIN0/D0	I	Analog Input 0/Data IO 0
8	AIN1/D1	I	Analog Input 1/Data IO 1
9	AIN4/D4	I	Analog Input 4/Data IO 4
10	AIN5/D5	I	Analog Input 5/Data IO 5
11	AIN6/D6	I	Analog Input 6/Data IO 6
12	AIN7/D7	I	Analog Input 7/Data IO 7
13	AIN2/D2	I	Analog Input 2/Data IO 2
14	AIN3/D3	I	Analog Input 3/Data IO 3
15	GND	-	Ground
16	$\overline{\text{CS}}$	I	Chip Select. Active Low
17	DIN	I	SPI Data Input
18	DOUT	O	SPI Data Output
19	SCLK	I	SPI Clock Input
20	$\overline{\text{DRDY}}$	O	Data Ready Indication Signal. Active Low

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	V_{DD}	-0.3 ~ 6	V
Input Current	I_{IN}	100 (Momentary)	mA
Input Current	I_{IN}	10 (Continuous)	mA
Analog Input Voltage	A_{IN}	-0.5 ~ V_{DD}+0.5	V
Digital Input Voltage	D_{IN}	-0.3 ~ V_{DD}+0.3	V
Digital Output Voltage	D_{OUT}	-0.3 ~ V_{DD}+0.3	V
Maximum Junction Temperature	J_T	150	°C
Operating Temperature	T_A	-40 ~ 85	°C
Storage Temperature	T_{STG}	-65 ~ 150	°C
Soldering Temperature(10s)		260	°C

ELECTRICAL CHARACTERISTICS

Digital Characteristics： T_{MIN} to T_{MAX}, V_{DD}: 2.7V to 5.25V.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Digital Input High-level Voltage	V_{IH}		0.8×V_{DD}		V_{DD}	V
Digital Input Low-level Voltage	V_{IL}		GND		0.2×V_{DD}	V
Digital Output High-level Voltage	V_{IH}	I_{OH} = 1mA	V_{DD} - 0.4			V
Digital Output Low-level Voltage	V_{IL}	I_{OL} = 1mA	GND		GND + 0.4	V
Input High-level Leakage Current	I_{IH}				10	µA
Input Lo -level Leakage Current	I_{IL}		-10			µA
Master Clock Frequency	f_{OSC}		1		5	MHz
Master Clock Period	t_{OSC}	1/f_{OSC}	200		1000	ns

Electrical Characteristics： T_{MIN} to T_{MAX}, V_{DD}=+5V, f_{MOD}=19.2kHz, PGA=1, Buffer on, f_{DATA}=15Hz, V_{REF}≡(V_{REFIN+})–($V_{REFIN–}$)= +2.5V.

Parameter	Condition	Min	Typ	Max	Unit
Analog Input					
Analog Input Range	Buffer Off	GND-0.1		V_{DD}+0.1	V
	Buffer On	GND+0.05		V_{DD}-1.5	V
Full-Scale Input Voltage	RANGE = 0			±V_{REF} /PGA	V
(A_{IN+}) - (A_{IN-})	RANGE = 1			±V_{REF} /(2×PGA)	V
Differential Input Impedance	Buffer Off		5/PGA		MΩ
	Buffer On		5		GΩ
Bandwidth (-3dB)	f_{DATA} = 3.75Hz		1.66		Hz
	f_{DATA} = 7.50Hz		3.44		Hz
	f_{DATA} = 15.0Hz		14.6		Hz
PGA	Selectable Gain Ranges	1		128	
Input Capacitance			9		pF
Input Leakage Current	Modulator Off, T = 25°C		5		pA
Burnout Current Source			2		µA
System Performance					
Resolution	No Missing Codes		24		Bits
Integral Non-linearity				±0.0015	% of FS
Offset Error			8ppm		of FS
Offset Error Drift			0.02ppm		of FS/°C
Gain Error			0.005		%
Gain Error Drift			1.0		ppm/°C

Parameter	Condition	Min	Typ	Max	Unit
Common-Mode Rejection	DC	100			dB
	f_{CM} = 60Hz, f_{DATA} =15Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 15Hz		120		dB
Notch Rejection	f_{CM} = 60Hz, f_{DATA} = 15Hz		100		dB
	f_{CM} = 50Hz, f_{DATA} = 15Hz		100		dB
Power Supply Rejection	DC	80	95		dB
Voltage Reference Voltage Input					
V_{REF}≡(V_{REF+})-(V_{REF-})	RANGE = 0	0.1	2.5	2.6	V
	RANGE = 1	0.1		V_{DD}	V
V_{REF+},V_{REF-} Input Range	RANGE = 0	0		V_{DD}	V
	RANGE = 1	0		V_{DD}	V
Common-mode Rejection	DC		120		dB
	f_{VREFCM} = 60Hz		120		dB
Bias Current	V_{REF} = 2.5V		1.3		μA
Offset DAC					
Offset DAC Range	RANGE = 0		±V_{REF}/ (2×PGA)		V
	RANGE = 1		±V_{REF}/ (4×PGA)		V
Monotonicity		8			Bits
Gain Error			±10		%
Gain Error Drift			1		ppm/°C
Power					
Power Supply	V_{DD}	4.75		5.25	V
Current	PGA = 1, Buffer Off		240	375	μA
	PGA = 128, Buffer Off		450	800	μA
	PGA = 1, Buffer On		290	425	μA
	PGA = 128, Buffer On		960	1400	μA
	SLEEP Mode		60		μA
	Read Data Continuous Mode		230		μA
	$\overline{PDWN}$= 0		0.5		nA
Current	PGA = 1, Buffer Off		240	375	μA
Power Dissipation	PGA = 1, Buffer Off		1.2	1.9	mW
Temperature Range					
Operating Temperature		-40		+85	°C

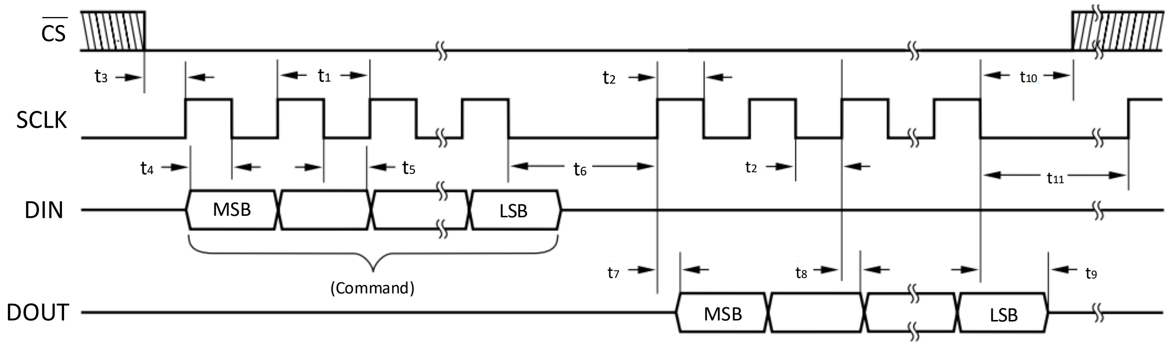
Electrical Characteristics : T_{MIN} to T_{MAX}, V_{DD} = +3V, f_{MOD} = 19.2kHz, PGA = 1, Buffer ON, f_{DATA} = 15Hz, V_{REF}≡(V_{REFIN+})–($V_{REFIN–}$) = +1.25V.

Parameter	Condition	Min	Typ	Max	Unit
Analog Input					
Analog Input Range	Buffer Off	GND-0.1		V_{DD}+0.1	V
	Buffer On	GND+0.05		V_{DD}-1.5	V
Full-Scale Input Voltage (A_{IN+}) - (A_{IN-})	RANGE = 0			±V_{REF} /PGA	V
	RANGE = 1			±V_{REF} /(2×PGA)	V
Differential Input Impedance	Buffer Off		5/PGA		MΩ
	Buffer On		5		GΩ
Bandwidth (-3dB)	f_{DATA} = 3.75Hz		1.66		Hz
	f_{DATA} = 7.50Hz		3.44		Hz
	f_{DATA} = 15.0Hz		14.6		Hz
PGA	Selectable Gain Ranges	1		128	
Input Capacitance			9		pF
Input Leakage Current	Modulator Off, T = 25°C		5		pA
Burnout Current Source			2		μA
System Performance					
Resolution	No Missing Codes		24		Bits
Integral Non-linearity				±0.0015	% of FS
Offset Error			15ppm		of FS
Offset Error Drift			0.04ppm		of FS/°C
Gain Error			0.01		%
Gain Error Drift			1.0		ppm/°C
Common-mode Rejection	DC	100			dB
	f_{CM} = 60Hz, f_{DATA} =15Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 15Hz		120		dB
Notch Rejection	f_{CM} = 60Hz, f_{DATA} = 15Hz		100		dB
	f_{CM} = 50Hz, f_{DATA} = 15Hz		100		dB
Power Supply Rejection	DC	75	90		dB
Voltage Reference Input					
V_{REF}≡(V_{REF+})-(V_{REF-})	RANGE = 0	0.1	1.25	1.26	V
	RANGE = 1	0.1	2.5	2.6	V
V_{REF+}, V_{REF-} Input Range	RANGE = 0	0		V_{DD}	V
	RANGE = 1	0		V_{DD}	V
Common-mode Rejection	DC		120		dB
	f_{VREFCM} = 60Hz		120		dB
Bias Current	V_{REF} = 1.25		0.65		μA

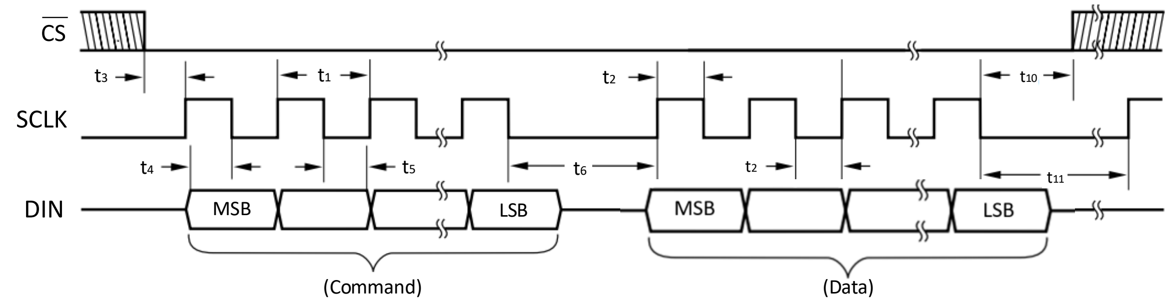
Parameter	Condition	Min	Typ	Max	Unit
Offset DAC					
Offset DAC Range	RANGE = 0		$\pm V_{REF}$/ (2×PGA)		V
	RANGE = 1		$\pm V_{REF}$/ (4×PGA)		V
Monotonicity		8			Bits
Gain Error			±10		%
Gain Error Drift			1		ppm/°C
Power					
Power Supply	V_{DD}	2.7		3.3	V
Current	PGA = 1, Buffer Off		190	375	μA
	PGA = 128, Buffer Off		460	700	μA
	PGA = 1, Buffer On		240	375	μA
	PGA = 128, Buffer On		870	1325	μA
	SLEEP Mode		75		μA
	Read Data Continuous Mode		1130		μA
	$\overline{PDWN}$ = 0		0.5		nA
Power Dissipation	PGA = 1, Buffer Off		0.6	1.2	mW
Temperature Range					
Operating Temperature		-40		+85	°C

FUNCTIONAL DESCRIPTION

1. Timing Diagrams

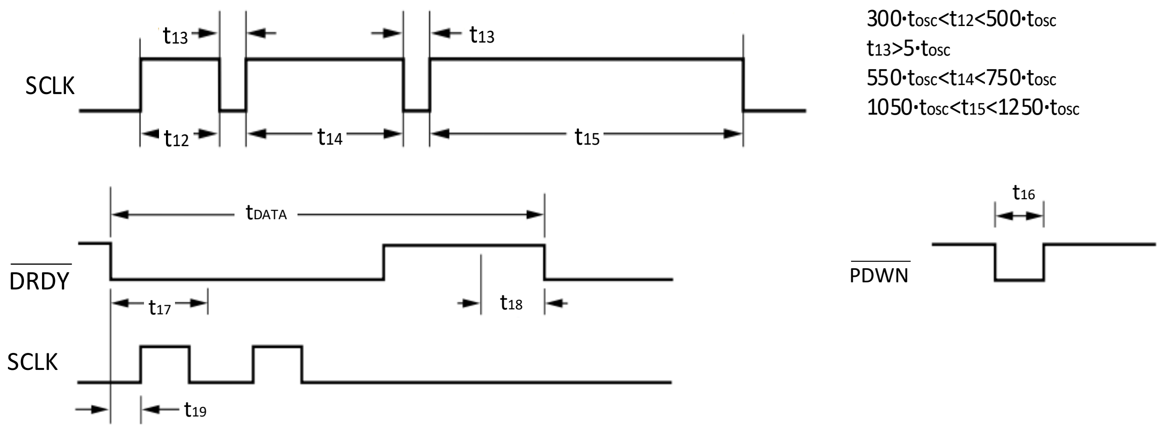


Read Timing Diagram



Write Timing Diagram

MS1242/MS1243 Reset on the Falling Edge



MS1242/MS1243 Timing Diagram

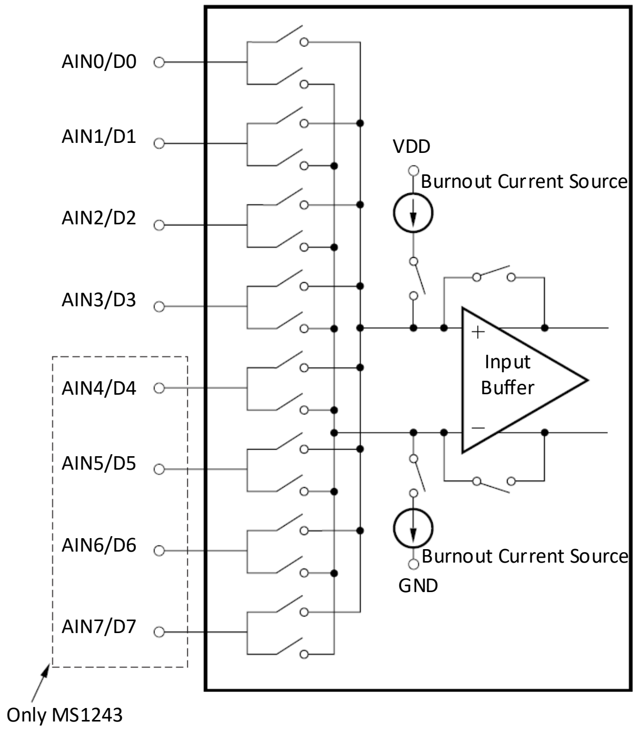
MS1242/MS1243 Timing Table

Parameter	Description		Min	Max	Unit
t_1	SCLK Period		4		t_{OSC}Period
				3	$\overline{DRDY}$Period
t_2	SCLK Pulse Width		200		ns
t_3	Setup Time, $\overline{CS}$ Falling Edge to First SCLK Edge		0		ns
t_4	Setup Time, DIN Valid to SCLK Edge		50		ns
t_5	Hold Time, DIN Valid to SCLK Edge		50		ns
t_6	Delay between the Last SCLK Edge for DIN and the First SCLK Edge for DOUT when sending RDATA, RDATAC and RREG Delay between the Last SCLK Edge for DIN and the First SCLK Edge for DIN when sending WREG		50		t_{OSC} Period
t_7	Delay between DOUT and SCLK			50	ns
t_8	Hold Time, SCLK Edge to DOUT		0		ns
t_9	Last SCLK Edge to DOUT Tri-State		6	10	t_{OSC} Period
t_{10}	Delay between the Final SCLK Edge and $\overline{CS}$ Signal End		0		ns
t_{11}	Final SCLK Edge of One Command until First Edge SCLK of Next Command	RREG, WREG, DSYNC, SLEEP, RDATA, RDATAC, STOPC	4		t_{OSC} Period
		OCALSYS, GCALSYS	8		$\overline{DRDY}$Period
		RESET	16		t_{OSC} Period
t_{16}	$\overline{PDWN}$ Pulse Width		4		t_{OSC} Period
t_{17}	Interval between $\overline{DRDY}$ Falling Edge and the Next Conversion Beginning(Allowed Analog Input Change)			5000	t_{OSC} Period
t_{18}	DOR Update Time (Reading DOR is Not Allowed)		4		t_{OSC} Period
t_{19}	First SCLK after $\overline{DRDY}$Goes Low	RDATAC Mode	10		t_{OSC} Period
t_{16}		Any Other Mode	0		t_{OSC} Period

2. Module Description

2.1 Input Multiplexer

The input multiplexer can provide any combination on any of the input channels, the schematic diagram is shown in the following figure.



The MS1242 has two pairs of differential inputs or three single-ended inputs at most. The MS1243 has four pairs of differential inputs or seven single-ended inputs at most. For example, if AIN1 is selected as the positive (negative) differential input, any other inputs can be selected as the negative (positive) terminals.

The MS1242 can switch input signal select and realize stable output of digital filter within single clock period. In order to decrease switch error, configure MUX register immediately after $\overline{\text{DRDY}}$signal goes low. The allowable operation time sees timing diagram t_{17}.

2.2 Burnout Current Sources

The Burnout current source can be used to detect sensor short-circuit or open-circuit conditions. The on or off is set by the Burnout Current Sources (BOCS) bit and the current is 2μA. When input sensor is shorted, Burnout current source makes the MS1242 output approximately zero. When input sensor is open-circuit, Burnout current source makes the MS1242 output approximately full-scale.

2.3 Input Buffer

The input impedance of the MS1242 without the enabled buffer is approximately 5MΩ/PGA. For systems requiring very high input impedance, the activated buffer raises the input impedance to approximately 5GΩ.

The buffer can be enabled using the ACR register. When the BUF bit in the ACR register is set to high, the input buffer is enabled and input impedance is effectively improved. If buffer is enabled, additional power dissipation is increased and it relates to PGA setting. When the PGA is set to 1, approximately 50μA current is increased; When the PGA is set to 128, up to 150μA current is increased. When buffer is enabled, the buffer's input range is from AGND+0.3V to AVDD-1.5V.

2.4 PGA

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can improve the effective resolution of the A/D converter.

2.5 Offset DAC

In order to extend input range, the MS1242 integrates an offset 8bit DAC. Offset DAC is a programmable voltage source. The input signal is magnified by PGA, then added up to ODAC output, and last input into Δ-Σ modulator.

2.6 Modulator

The modulator of the MS1242 is a single-loop and 2th-order delta-sigma modulator. The sample frequency is controlled by the SPEED bit (ACR bit5), as shown in the following table.

Crystal Frequency (MHz)	Speed	ADC Sampling Frequency (kHz)	Data Output Rate(Hz)			Notch Frequency (Hz)
			00	01	10	
2.4576	0	19.200	15	7.5	3.75	50/60
	1	9.600	7.5	3.75	1.875	25/30
4.9152	0	38.400	30	15	7.5	100/120
	1	19.200	15	7.5	3.75	50/60

2.7 Calibration

The MS1242 calibration includes self and system calibration. Calibration includes offset calibration and gain calibration.

Self-calibration is handled by three commands: SELFCAL, SELFGAL, and SELFOCAL. Each calibration takes two data conversion periods. During self-calibration, the ADC turns off external input terminals. The PGA must be set to 1 prior to issuing a SELFCAL or SELFGCAL command. When input reference voltage is greater than VDD–1.5V, the buffer must be turned off.

System calibration can correct both offset error and gain errors. Calibration must be performed after the correct input signal. The system offset calibration command (SYSOCAL) requires zero input differential signal. It then computes the offset that nullifies the offset into the OCR register. The system gain calibration command (SYSGCAL) requires positive full-scale input signal. It then computes a value to nullify the gain error into the FSR register. Each calibration takes two data conversion periods.

Error calibration should be performed after power on, temperature change or PGA change. The RANGE bit (ACR bit2) must be set to zero and the offset DAC is disabled during calibration. At the completion of calibration, the $\overline{\text{DRDY}}$signal goes low. The first output data after calibration should be discarded.

2.8 External Reference Voltage

The MS1242 requires an external voltage reference. The reference voltage value is selected by the ACR register. Voltage reference is connected between the pins: VREF+ and VREF–, and the voltage should not more than VDD.

For VDD = 5.0V and RANGE = 0, the differential VREF must not exceed 2.5V.

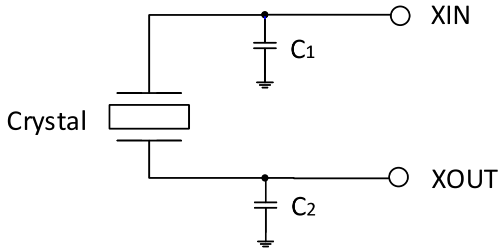
For VDD = 5.0V and RANGE = 1, the differential VREF must not exceed 5V.

For VDD = 3.0V and RANGE = 0, the differential VREF must not exceed 1.25V.

For VDD = 3.0V and RANGE = 1, the differential VREF must not exceed 2.5V.

2.9 Clock Generator

The clock source for the MS1242 can be provided from a crystal, oscillator or clock. When the clock source is connected externally, it is connected with XIN pin and XOUT pin is NC. When the clock source is a crystal, external capacitors (10pF~20pF) must be provided on XIN and XOUT pin, as shown in the following figure.



2.10 Digital Filter

The MS1242 has a programmable Finite Impulse Response (FIR) filter that be configured as various output data rates. When a 2.4576MHz clock is used, the output data rate can be configured as 15Hz, 7.5Hz or 3.75Hz. Under these conditions, the FIR filter rejects both 50Hz and 60Hz interference.

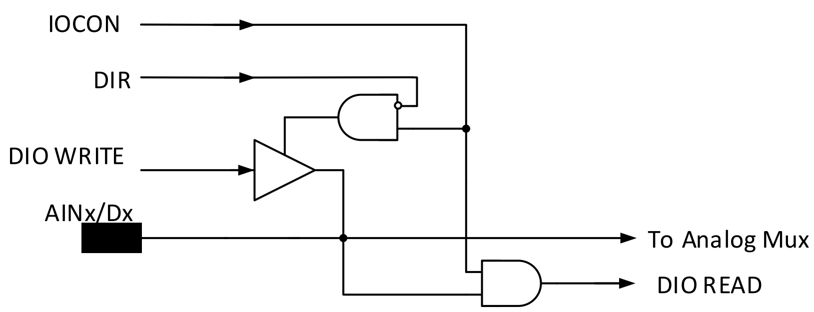
If other output data rates are desired, other clock frequencies can be used. However, the rejection frequencies shift accordingly. For example, a 3.6864MHz master clock with the default register condition has:

Output Data Rate: (3.6864MHz/2.4576MHz) ×15Hz = 22.5Hz

The First and Second Notch: (3.6864MHz/2.4576MHz) × (50Hz and 60Hz) = (75Hz and 90Hz)

2.11 Data I/O Interface

The data interface provides a dual purpose as both analog input and data I/O. The interface is configured by IOCON, DIR, and DIO register. The default configuration of power on is analog input. The equivalent schematic can be seen blow:



2.12 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) allows a controller to communicate with the MS1242.The MS1242/MS1243 operates only in slave mode. The serial interface is a standard four-wire SPI ($\overline{CS}$, SCLK, DIN and DOUT) interface.

2.12.1 Chip Select ($\overline{CS}$)

The chip select ($\overline{CS}$) input must be first issued before communicating with the MS1242/MS1243 . $\overline{CS}$ must stay low for the duration of the communication. When $\overline{CS}$ goes high, the serial interface is reset. $\overline{CS}$ also can be hard-wired low.

When $\overline{CS}$ signal stay constant low, the serial interface can operate in three-wire mode. The condition is appropriate for communication between MS1242 and external microcontroller.

2.12.2 Serial Clock (SCLK)

The serial clock (SCLK) is built in Schmitt trigger. If SCLK doesn't occur within three $\overline{DRDY}$periods, the SPI would be reset on the next SCLK and starts a new communication cycle. A special pattern on SCLK resets the entire chip.

2.12.3 Data Input (DIN) and Data Output (DOUT)

The data input (DIN) and data output (DOUT) are used to input and output data. DOUT is high impedance when not in use to allow DIN and DOUT to be connected together and driven by a bidirectional bus. Note: the Read Data Continuous Mode (RDATAC) command should not be issued in this condition. Because RDATAC command needs STOPC or RESET command to end. However, in RDATAC mode, the bidirectional bus is occupied by DOUT to send data all time. So STOPC or RESET command cannot be sent to the MS1242/MS1243 by bus. At this time, DIN would detect STOPC or RESET command to finish RDATAC state or reset.

2.13 Data Ready ($\overline{DRDY}$)

The Data Ready ($\overline{DRDY}$) indicates the date of internal data register. When data is ready to be read from the internal data register. $\overline{DRDY}$goes low when a new data is available in the DOR register. It goes high when DOR read operation is completed. It also goes high before updating the data in the DOR register to indicate the data is not available at this time, in order to avoid reading data from DOR register, as shown timing diagram t18.

The status of $\overline{DRDY}$can also be obtained by bit 7 of the ACR register.

2.14 Data Synchronization(DSYNC)

Synchronization can be achieved through the DSYNC command. When the DSYNC command is sent, the digital filter is reset on the edge of the last SCLK of the DSYNC command. And the modulator is also in reset state. Synchronization occurs on the next rising edge of the system clock after the first SCLK following the DSYNC command.

2.15 Supply Voltage Ramp Rate

The power-on reset circuitry is designed to compatible with digital supply as slow as 1V/10ms. To ensure normal operation, power supply should rise monotonically.

3. Registers Description

The operation of the MS1242/MS1243 is configured by registers.

3.1 Registers table

The MS1242/MS1243 registers are shown in blow table

Add	Reg	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H	SETUP	ID	ID	ID	ID	BOCS	PGA2	PGA1	PGA0
01H	MUX	PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0
02H	ACR	$\overline{\text{DRDY}}$	U/B	SPEED	BUFEN	BIT ORDER	RANGE	DR1	DR0
03H	ODAC	SIGN	OSET6	OSET5	OSET4	OSET3	OSET2	OSET1	OSET0
04H	DIO	DIO_7	DIO_6	DIO_5	DIO_4	DIO_3	DIO_2	DIO_1	DIO_0
05H	DIR	DIR_7	DIR_6	DIR_5	DIR_4	DIR_3	DIR_2	DIR_1	DIR_0
06H	IOCON	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
07H	OCR0	OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00
08H	OCR1	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08
09H	OCR2	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
0AH	FSR0	FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00
0BH	FSR1	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08
0CH	FSR2	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16
0DH	DOR2	DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16
0EH	DOR1	DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08
0FH	DOR0	DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00

3.2 Detailed Register Definition

SETUP Register (Address=00H, Reset Value=X0H)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ID	ID	ID	ID	BOCS	PGA2	PGA1	PGA0

SETUP. 7-4 : ID Number, Factory Programmed Bits

SETUP. 3 : BOCS: Burnout Current Source

0 = Disabled (default)； 1 = Enabled

SETUP. 2-0：PGA2~0: Programmable Gain Amplifier

000 = 1 (default)
001 = 2
010 = 4
011 = 8
100 = 16
101 = 32
110 = 64
111 = 128

MUX Register (Address=01H, Reset Value=01H)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0

MUX. 7-4 : PS3 ~ 0, Positive Channel Selection

0000 = AIN0 (default)
0001 = AIN1
0010 = AIN2
0011 = AIN3
0100 = AIN4
0101 = AIN5
0110 = AIN6
0111 = AIN7
Other = Reserved

MUX. 3-0 : NS3 ~ 0, Negative Channel Selection

0000 = AIN0
0001 = AIN1 (default)
0010 = AIN2
0011 = AIN3
0100 = AIN4
0101 = AIN5
0110 = AIN6
0111 = AIN7
Other = Reserved

ACR Register (Address=02H, Reset Value=00H)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$\overline{\text{DRDY}}$	U/B	SPEED	BUFEN	BIT ORDER	RANGE	DR1	DR0

ACR.7 : $\overline{\text{DRDY}}$, Data Ready (Read Only) . This bit duplicates the state of the $\overline{\text{DRDY}}$pin.

ACR.6 : U/B , Unipolar/Bipolar Select

0 = Bipolar (default)
1 = Unipolar

ACR.5 : SPEED, Modulator Clock Speed

0 = f_{OSC}/128 (default)
1 = f_{OSC}/256

ACR.4 : BUFEN, Buffer Enable

0 = Buffer Disabled (default)
1 = Buffer Enabled

ACR.3 : BITOR, Data Output Bit Order

0 = Most Significant Bit Transmitted First (default)
1 = Least Significant Bit Transmitted First

ACR.2 :	RANGE, Range Select 0 = Full-Scale Input Range equal to ±VREF (default) 1 = Full-Scale Input Range equal to ± VREF/2
ACR.1-0 :	DR1/DR0, Data Rate 00 = 15Hz (default) 01 = 7.5Hz 10 = 3.75Hz 11 = Reserved

ODAC Register (Address=03H, Reset Value=00H)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SIGN	OSET6	OSET5	OSET4	OSET3	OSET2	OSET1	OSET0

ODAC.7 : Sign Bit, 0 = Positive, 1 = Negative

ODAC.6-0 : Offset Value

DIO Register (Address=04H, Reset Value=00H)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DIO_7	DIO_6	DIO_5	DIO_4	DIO_3	DIO_2	DIO_1	DIO_0

If the IOCON register is configured as digital data mode. And DIR register is configured as output. Reading this register returns the value of the data I/O pins.

DIR Register (Address= 05H, Reset Value=FFH)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DIR_7	DIR_6	DIR_5	DIR_4	DIR_3	DIR_2	DIR_1	DIR_0

Each bit controls whether the corresponding data I/O pin is an output (= 0) or input (= 1).

The default power-up state is as inputs.

IOCON Register (Address=06H, Reset Value=00H)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0

IOCON. 7-0: I/O Configuration

0 = Analog (default)

1 = Digital

Bits 4 to 7 are not used in the MS1242.

OCR0 Register (Address=07H, Reset Value=00H)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

OCR1 Register (Address=08H, Reset Value=00H) Offset Calibration Coefficient

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08

OCR2 Register (Address=09H, Reset Value=00H) Offset Calibration Coefficient

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16

FSR0 Register(Address=0AH, Reset Value=59H) Offset Calibration Coefficient

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00

FSR1 Register(Address=0BH, Reset Value=55H) Gain Calibration Coefficient

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08

FSR2 Register (Address=0CH, Reset Value=55H) Gain Calibration Coefficient

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

DOR2 Register (Address=0DH, Reset Value=00H) Data Output Register

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16

DOR1 Register (Address=0EH, Reset Value=00H) Data Output Register

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08

DOR0 Register (Address=0FH, Reset Value=00H) Data Output Register

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00

4. MS1242/MS1243 Command Definitions

The MS1242/MS1243 uses a series of commands. Some of the commands are stand-alone commands (such as RESET), while others require additional operands (such as WREG).

Operands:

n = count (0 to 127)

r = register (0 to 15)

x = don't care

Command Summary

Commands	Description	Op Code	2nd Command Byte
RDATA	Read Data	00000001(01H)	—
RDATAC	Read Data Continuously	00000011(03H)	—
STOPC	Stop Read Data Continuously	00001111(0FH)	—
RREG	Read from REG "rrrr"	0001rrrr(1rH)	xxxx_nnnn(#of regs-1)
WREG	Write to REG "rrrr"	0101rrrr(5rH)	xxxx_nnnn(#of regs-1)
SELFCAL	Offset and Gain Self Cal	11110000(F0H)	—
SELFOCAL	Self Offset Cal	11110001(F1H)	—
SELFGCAL	Self Gain Cal	11110010(F2H)	—
SYSOCAL	Sys Offset Cal	11110011(F3H)	—
SYSGCAL	Sys Gain Cal	11110100(F4H)	—
WAKEUP	Wakeup	11111011(FBH)	—
DSYNC	Sync $\overline{DRDY}$	11111100(FCH)	—
SLEEP	Sleep	11111101(FDH)	—
RESET	Reset	11111110(FEH)	—

NOTE: The received data format is always MSB first. Data output format is set by ORDER bit.
of regs-1 represents that the count of required registers needs to decrease 1.

RDATA-Read Data

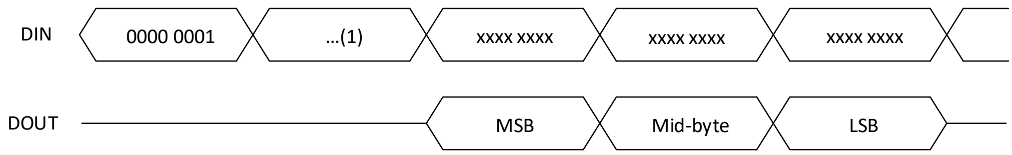
Description: Read the newest conversion result from Data Output Register (DOR). This is a 24-bit value.

Operands: None

Bytes: 1

Encoding: 0000 0001

Data Transfer Sequence:



NOTE : (1) For wait time, refer to timing specification.

RDATAC-Read Data Continuous

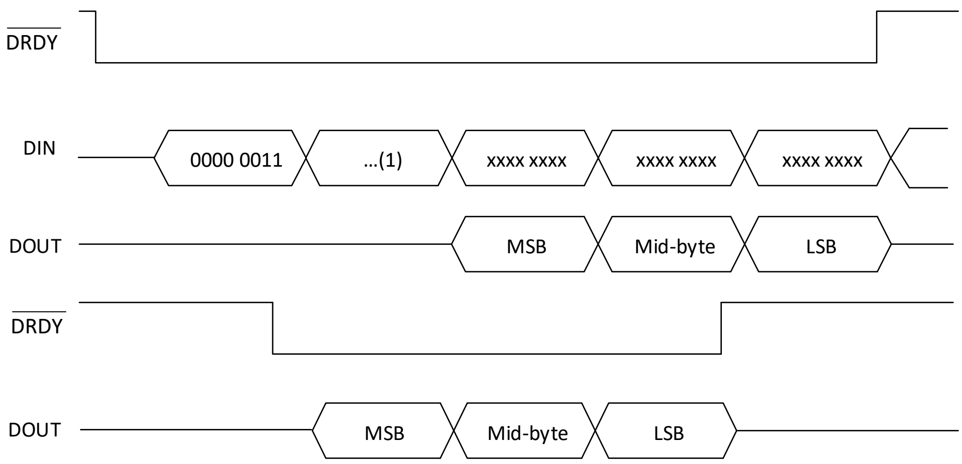
Description: Read Data Continuous mode enables the continuous read conversion results from DOR register on each $\overline{DRDY}$ period. This mode may be terminated by either the STOPC command or the RESET command. Wait at least 10 f_{OSC} after $\overline{DRDY}$ falls before reading.

Operands: None

Bytes: 1

Encoding: 0000 0011

Data Transfer Sequence:



NOTE : (1) For wait time, refer to timing specification.

STOPC-Stop Continuous

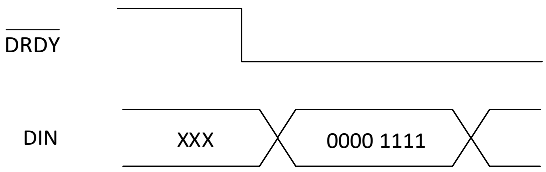
Description: Ends the continuous data output mode. Issue after $\overline{DRDY}$ goes low.

Operands: None

Bytes: 1

Encoding: 0000 1111

Data Transfer Sequence:



RREG-Read from Registers

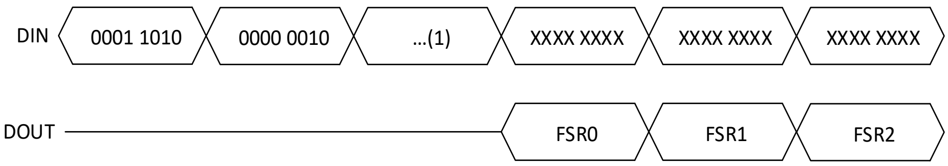
Description: Output the data from up to 16 registers starting with the register address specified as first operand of the instruction. The number of registers will be one plus the second byte count. If the count exceeds the remaining registers, the addresses wrap back to the beginning.

Operands: r, n

Bytes: 2

Encoding: 0001 rrrr xxxx nnnn

Data Transfer Sequence: Read FSR Starting from Register 0AH, three bytes. The first byte is 1AH (0001_1010) and is consist of RREG command and address 0AH. The second byte is 02H (length 3-1=2).



NOTE : (1) For wait time, refer to timing specification.

WREG-Write to Registers

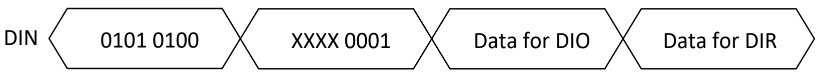
Description: Write to the registers starting with the register address specified as first operand of the instruction. The number of registers that will be written is one plus the value of the second byte.

Operands: r, n

Bytes: 2

Encoding: 0101 rrrr xxxx nnnn

Data Transfer Sequence: Write Two Registers Starting from 04H (DIO)



SELFCAL-Offset and Gain Self Calibration

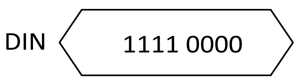
Description: The Offset Calibration Register (OCR) and the Full-Scale Register (FSR) are updated with calibration result.

Operands: None

Bytes: 1

Encoding: 1111 0000

Data Transfer Sequence:



SELFOCAL-Offset Self Calibration

Description: The Offset Calibration Register (OCR) is updated with calibration result.
Operands: None
Bytes: 1
Encoding: 1111 0001

Data Transfer Sequence: DIN ⟨ 1111 0001 ⟩

SELFGCAL-Gain Self Calibration

Description: The Full-Scale Register (FSR) is updated with calibration result.
Operands: None
Bytes: 1
Encoding: 1111 0010

Data Transfer Sequence: DIN ⟨ 1111 0010 ⟩

SYSOCAL-System Offset Calibration

Description: System offset calibration. The input should be set to 0V, and the MS1242/MS1243 computes the OCR value that compensates for offset errors. The Offset Calibration Register (OCR) is updated after this operation.
Operands: None
Bytes: 1
Encoding: 1111 0011

Data Transfer Sequence: DIN ⟨ 1111 0011 ⟩

SYSGCAL-System Gain Calibration

Description: System gain calibration. At this time, system input signal should be full-scale voltage. The MS1242/MS1243 computes the FSR value that will compensate for gain errors. The FSR is updated after this operation.
Operands: None
Bytes: 1
Encoding: 1111 0100

Data Transfer Sequence: DIN ⟨ 1111 0100 ⟩

WAKEUP

Description: Wakes the MS1242/MS1243 from SLEEP mode.

Operands: None

Bytes: 1

Encoding: 1111 1011

Data Transfer Sequence: DIN 1111 1011

DSYNC-Sync $\overline{\text{DRDY}}$

Description: Synchronize the MS1242/MS1243.

Operands: None

Bytes: 1

Encoding: 1111 1100

Data Transfer Sequence: DIN 1111 1100

SLEEP-Sleep Mode

Description: Make the MS1242/MS1243 into sleep mode. To exit sleep mode, use WAKEUP command.

Operands: None

Bytes: 1

Encoding: 1111 1101

Data Transfer Sequence: DIN 1111 1101

RESET-Reset to Default Values

Description: Reset the registers to power-up values. This command stops the Read Continuous mode.

Operands: None

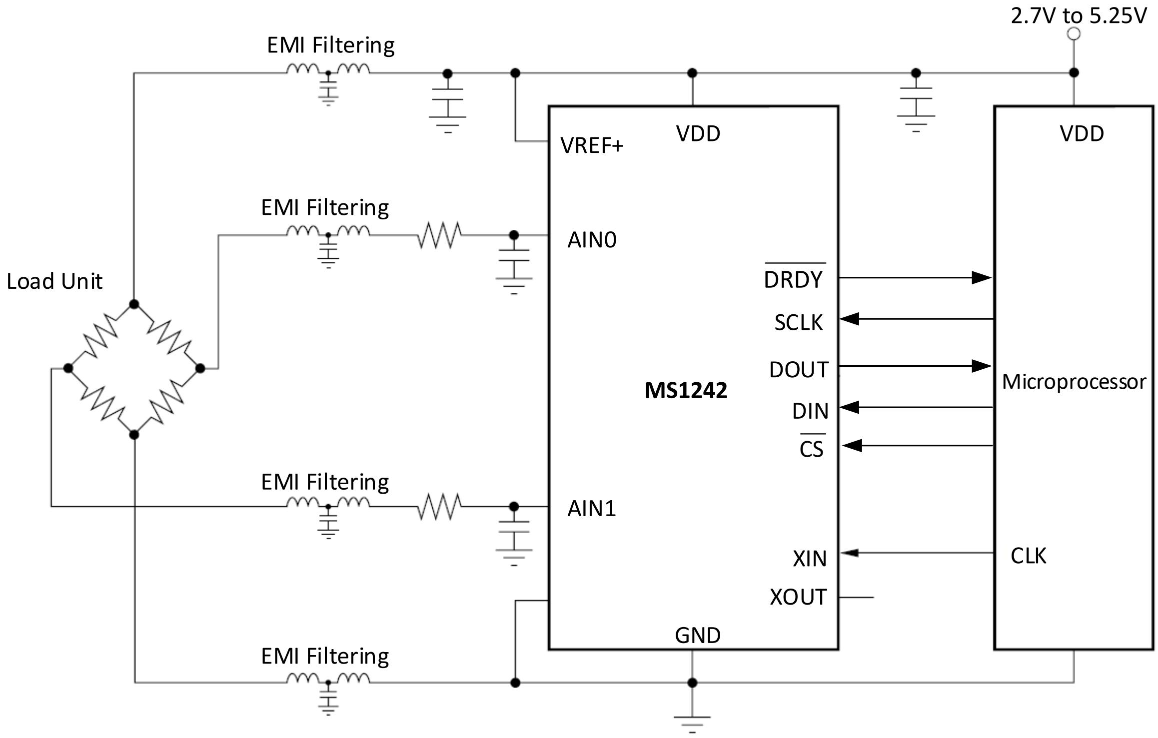
Bytes: 1

Encoding: 1111 1110

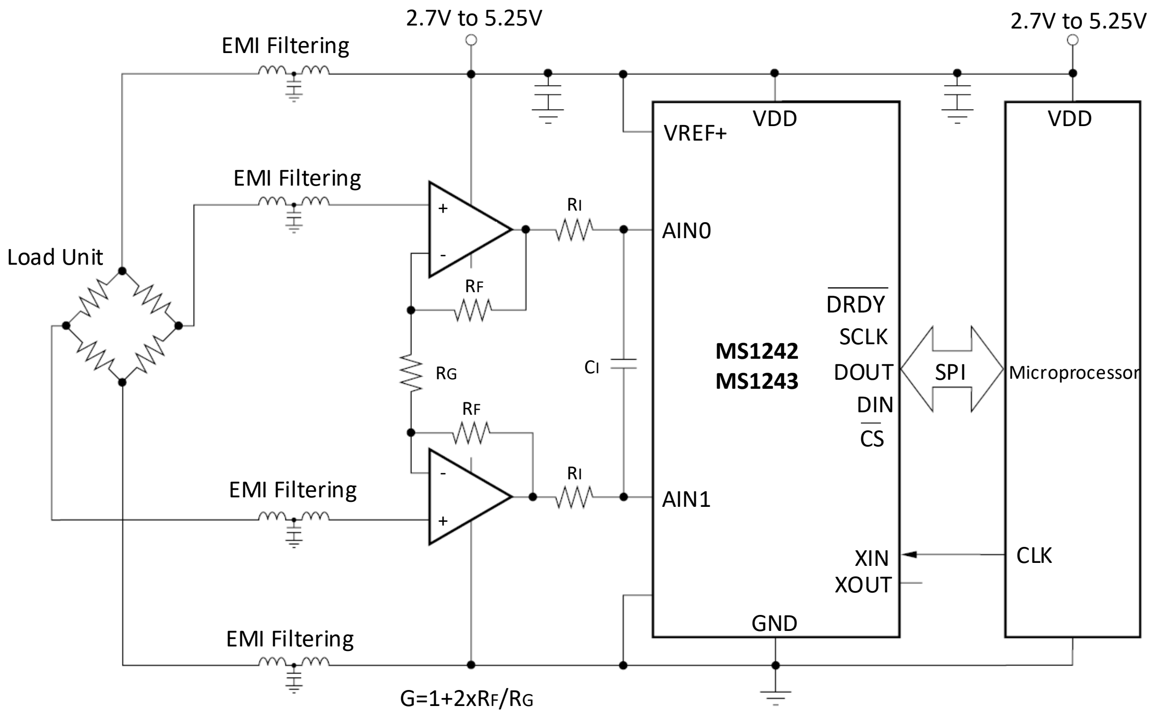
Data Transfer Sequence: DIN 1111 1110

TYPICAL APPLICATION DIAGRAM

The diagram below shows a typical application diagram of general weight scale using the MS1242.

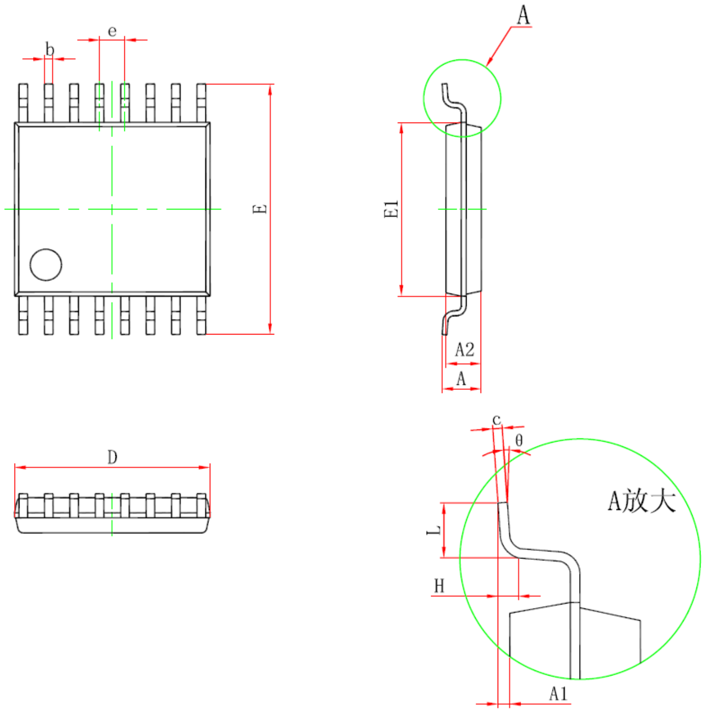


The diagram below shows a typical application` diagram of high-precision weight scale using the MS1242 /MS1243.



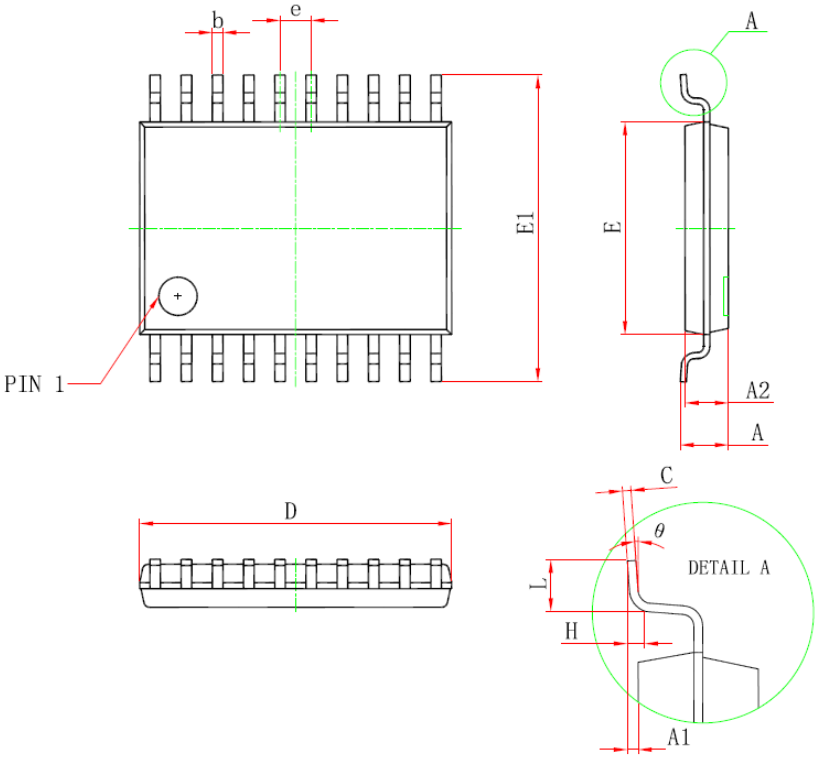
PACKAGE OUTLINE DIMENSIONS

TSSOP16



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
E	6.250	6.550	0.246	0.258
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	4.300	4.500	0.169	0.177
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

TSSOP20



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name : MS1242, MS1243

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS1242	TSSOP16	3000	1	3000	8	24000
MS1243	TSSOP20	3000	1	3000	8	24000

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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