

MS90C366

——+3.3V 175MHz 18bits COLOR LVDS Receiver

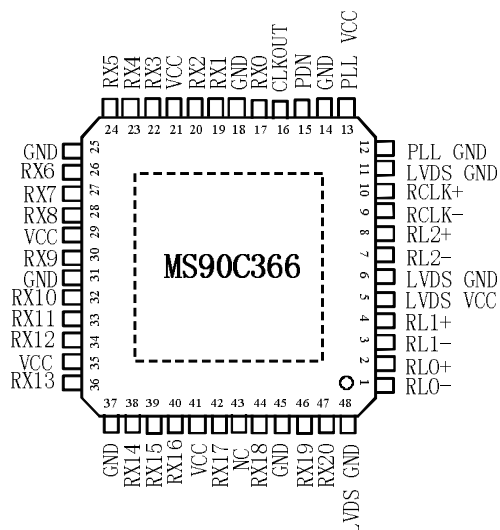
General Description

The MS90C366 receiver is designed to support pixel data transmission between Host and Flat Panel Display from NTSC up to SXGA resolutions. The MS90C366 converts the LVDS data streams back into 21bits of CMOS/TTL data with the choice of the rising edge or falling edge clock for the convenience with a variety of LCD panel controllers. At a transmit clock frequency of 175Mhz, 18bits of GRB data and 3bits of timing and control data (HSYNC,VSYCN,DE) are transmitted at an effective rate of 1225Mbps per LVDS channel. Using a 175MHz clock, the data throughput is 459.3Mbytes/sec.

Features

- Clock range: 8-175MHz
- Narrow bus reduces cable size
- Single 3.3V supply
- Power-down Mode
- Supports VGA、SVGA、XGA、SXGA
- Up to 3.675Gbps throughput
- Up to 459.3Megabytes/sec bandwidth
- PLL requires no external components
- Compatible with TIA/EIA-644 LVDS standard
- LQFP48 Package

Pin Diagram

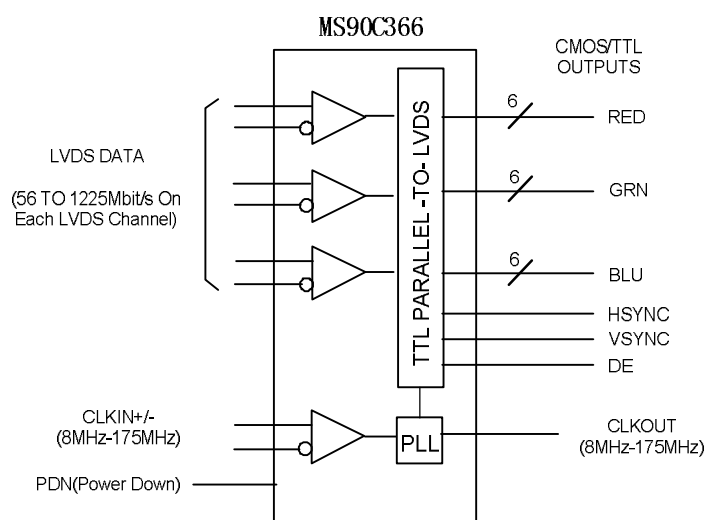


Pin Description

Pin Name	Pin No.	I/O	Description
RxIN0+, RxIN0-	2, 1	LVDS IN	LVDS differential data inputs
RxIN1+, RxIN1-	4, 3	LVDS IN	
RxIN2+, RxIN2-	8, 7	LVDS IN	
RxCLKIN+, RxCLKIN-	10, 9	LVDS IN	LVDS differential clock inputs
RxOUT0 ~ RxOUT6	17, 19, 20, 22, 23, 24, 26	OUT	TTL level data outputs. This includes: 6 RED, 6 GREEN, 6 BLUE, 3 control lines (HSYNC, VSYNC, DE)
RxOUT7 ~ RxOUT13	27, 28, 30, 32, 33, 34, 36	OUT	
RxOUT14 ~ RxOUT20	38, 39, 40, 42, 44, 46, 47	OUT	
CLKOUT	16	OUT	TTL level clock output.
PDN	25	IN	TTL level input. H: Normal operation L: Power down
Vcc	21, 29, 35, 41	Power	Power supply pins for TTL outputs.
GND	14, 18, 25, 31, 37, 45	Ground	Ground pins for TTL outputs.
LVDS Vcc	5	Power	Power supply pins for LVDS

			inputs.
LVDS GND	6, 11, 48	Ground	Ground pins for LVDS inputs.
PLL Vcc	13	Power	Power supply for PLL.
PLL GND	12	Ground	Ground pins for PLL.
NC	43	--	NC

Block Diagram



Absolute Maximum Ratings

Supply Voltage (VCC)	-0.3V - 4.0V
CMOS/TTL Input Voltage	-0.3V - (VCC+0.3V)
CMOS/TTL Output Voltage	-0.3V - (VCC+0.3V)
LVDS Input Voltage	-0.3V - (VCC+0.3V)
Junction Temperature	+150°C
Storage Temperature	-40°C - 100°C
Lead Temperature(Soldering,4 sec)	+260°C
Maximum Power Dissipation Capacity (25°C)	
MS90C366	1.2W

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	$I_{OH} = -4mA$ (data) $I_{OH} = -8mA$ (clock)	2.4			V
V_{OL}	Low Level Output Voltage	$I_{OL} = 4mA$ (data) $I_{OL} = 8mA$ (clock)		0.06	0.3	V
I_{IN}	Input Current	$0 \leq V_{IN} \leq V_{CC}$			± 10	μA
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0V$			-50	mA

DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	$V_{OC} = +1.2V$			+100	mV
V_{TL}	Differential Input Low Threshold		-100			mV
I_{IN}	Input Current	$V_{IN} = +2.4V/0V, V_{CC} = 3.6V$			± 10	μA

SUPPLY CURRENT

Symbol	Parameter	Conditions	Typ	Max	Units
ICC_{RG}	Supply Current (16 Grayscale)	$CL = 8pF, f = 90MHz, V_{CC} = 3.3V$ 16 Grayscale Pattern	60	71	mA
ICC_{RW}	Supply Current (Worst Case)	$CL = 8pF, f = 90MHz, V_{CC} = 3.3V$ Worst Case Pattern	96	102	mA
ICC_{RP}	Supply Current (Power Down)	PDN=0V		10	μA

Switching Characteristics

Symbol	Parameter	Min	Typ	Max	Units
T_{RCP}	CLKOUT Period	11.1	T	125	ns
T_{RCH}	CLKOUT High Time		T/2		ns
T_{RCL}	CLKOUT Low Time		T/2		ns
T_{RS}	TTL Data Setup to CLKOUT	5.0			ns

T _{RH}	TTL Data Hold from CLKOUT		1.0			ns
T _{TLH}	TTL Low to High Transition Time			2	3	ns
T _{THL}	TTL High to Low Transition Time			2	3	ns
T _{RCD}	RCLK to CLKOUT Delay			7.0		ns
T _{RDP5}	Position 0	175MHz	−0.4	0	+0.4	ns
T _{RDP6}	Position 1		T/7−0.4	T/7	T/7+0.4	ns
T _{RDP0}	Position 2		2T/7−0.4	2T/7	2T/7+0.4	ns
T _{RDP1}	Position 3		3T/7−0.4	3T/7	3T/7+0.4	ns
T _{RDP2}	Position 4		4T/7−0.4	4T/7	4T/7+0.4	ns
T _{RDP3}	Position 5		5T/7−0.4	5T/7	5T/7+0.4	ns
T _{RDP4}	Position 6		6T/7−0.4	6T/7	6T/7+0.4	ns
T _{TPLLS}	PLL Set		−	−	10	ms

AC Timing Diagram

FIGURE 1. Test Pattern “Worst Case Pattern”

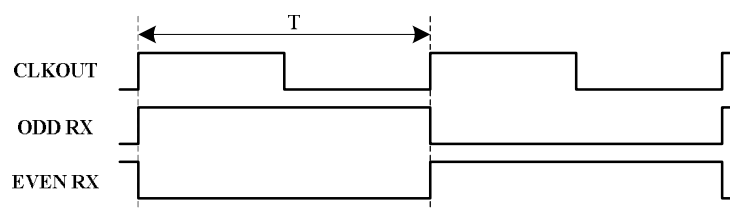


FIGURE 2. Test Pattern “16 Grayscale Test Pattern”

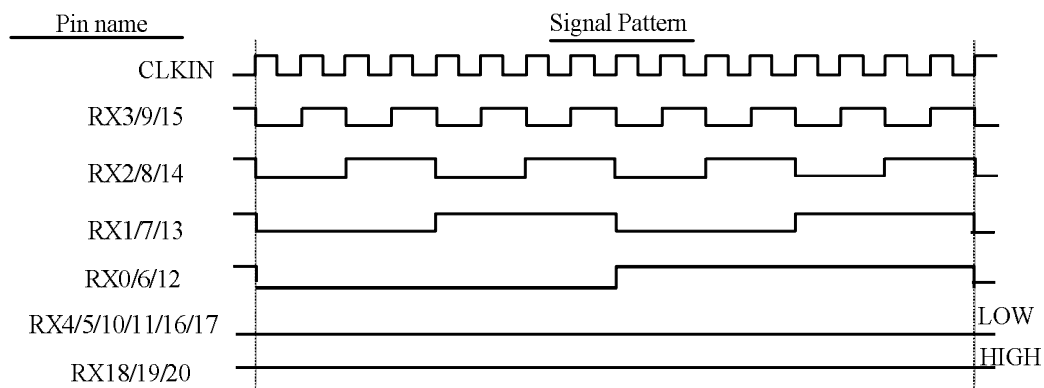


FIGURE 3. TTL Output

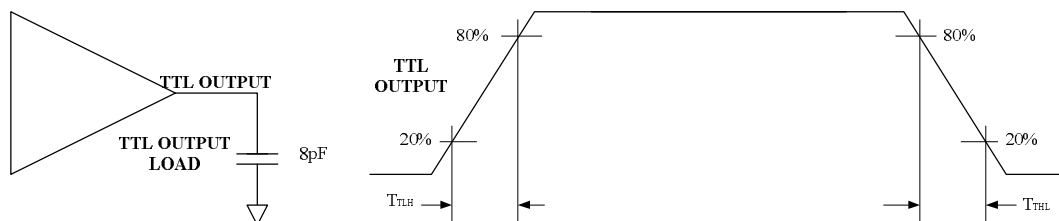


FIGURE 4. PLL Set Time

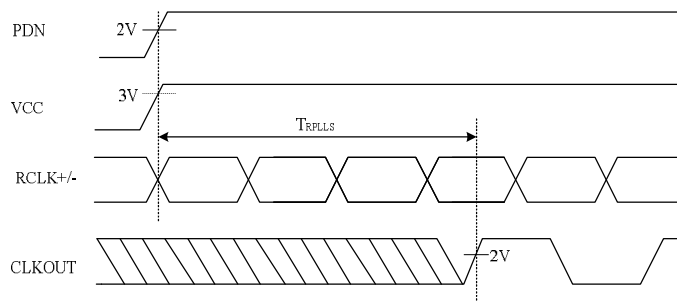
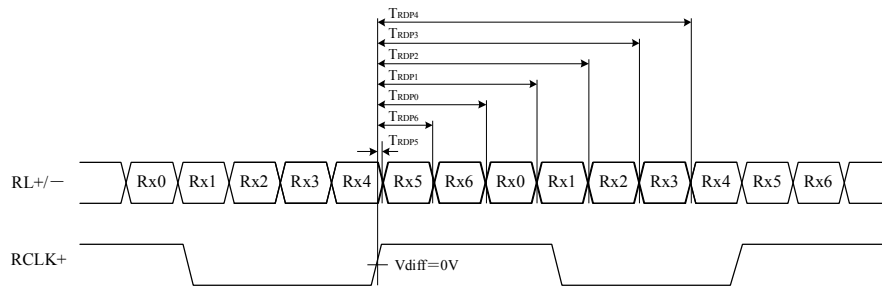


FIGURE 5. Receiver Device Operation



$$V_{diff} = (R_{xIN+}) - (R_{xIN-}), \dots, (R_{xCLKIN+}) - (R_{xCLKIN-})$$

FIGURE 6. LVDS Inputs Mapped Parallel TTL Data Outputs

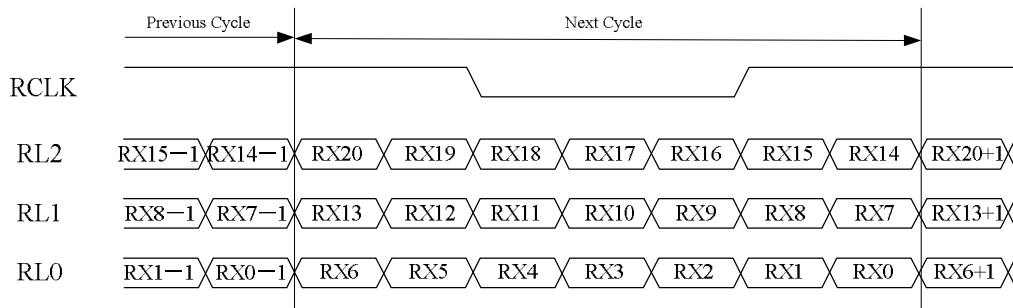


FIGURE 7. Setup/Hold and High/Low Times

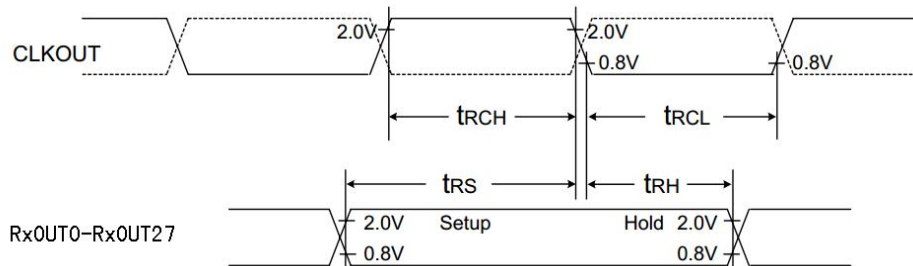
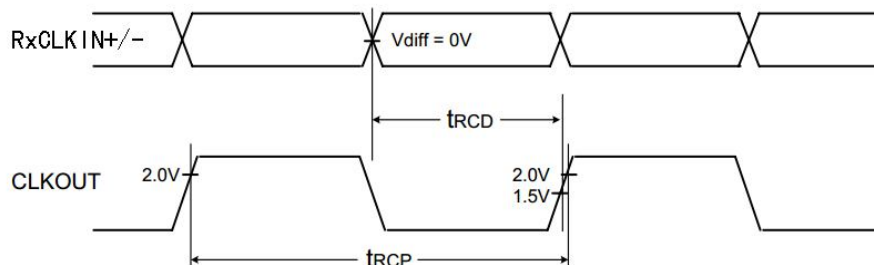


FIGURE 8. RCLK to CLKOUT Delay



Package

Symbol	Min	Nom	Max
A	1.10	1.15	1.20
A1	0.01	—	0.21
A2	0.9	1.0	1.1
E3	—	0.254	—
b	0.15	0.2	0.25
b1	0.16	0.22	0.28
c	—	0.127	—
D1	6.85	6.95	7.05
D2	6.9	7.00	7.10
E	8.8	9.00	9.20
E1	6.85	6.95	7.05
E2	6.9	7.00	7.10
E3	—	0.5	—
L	0.43	—	0.71
L1	0.90	1.0	1.10
R	0.1	—	0.25
R1	0.1	—	—
θ	0	—	10°
θ1	0	—	—
γ	—	—	0.1
Z	—	0.75	—

