+3.3V, 145 MHz, 24-Bit LVDS Flat Panel Display Transmitter

PRODUCT DESCRIPTION

The MS90C385B transmitter converts 28 bits TTL data to four-channel LVDS (Low Voltage Differential Signaling). Clock channel is phase-locked and then is in parallel with data channel. When clock frequency is 145MHz, 24 bits of RGB data and 3 bits of LCD timing data and 1bit control data are transmitted at a rate of 1015Mbps per LVDS data channel. When input clock frequency is 145MHz, the data transmit rate is 507.5Mbytes/sec. The MS90C385B can be programmed as valid for clock rising edge or falling edge via R_FB pin. The MS90C385B is an ideal product to solve EMI and cable length problems associated with wide bandwidth, high-speed TTL signal.

TSSOP56

FEATURES

- Frequency Range: 20-145MHz Clock Signal
- Less Bus Reducing Cable Size and Cost
- IO Power Supply Compatible with 1.8V, 3.3V
- Low Power Dissipation Mode
- Support VGA, SVGA, XGA, SXGA
- Support Extend Frequency Spectrum Clock Generation
- Internal Integrated Input Jitter Filter
- 507.5 Megabytes/sec Bandwidth
- Reduced LVDS Swing to Reduce EMI (200mV or 345mV Optional)
- PLL without External Structure
- Observe TIA/EIA-644 LVDS Standard

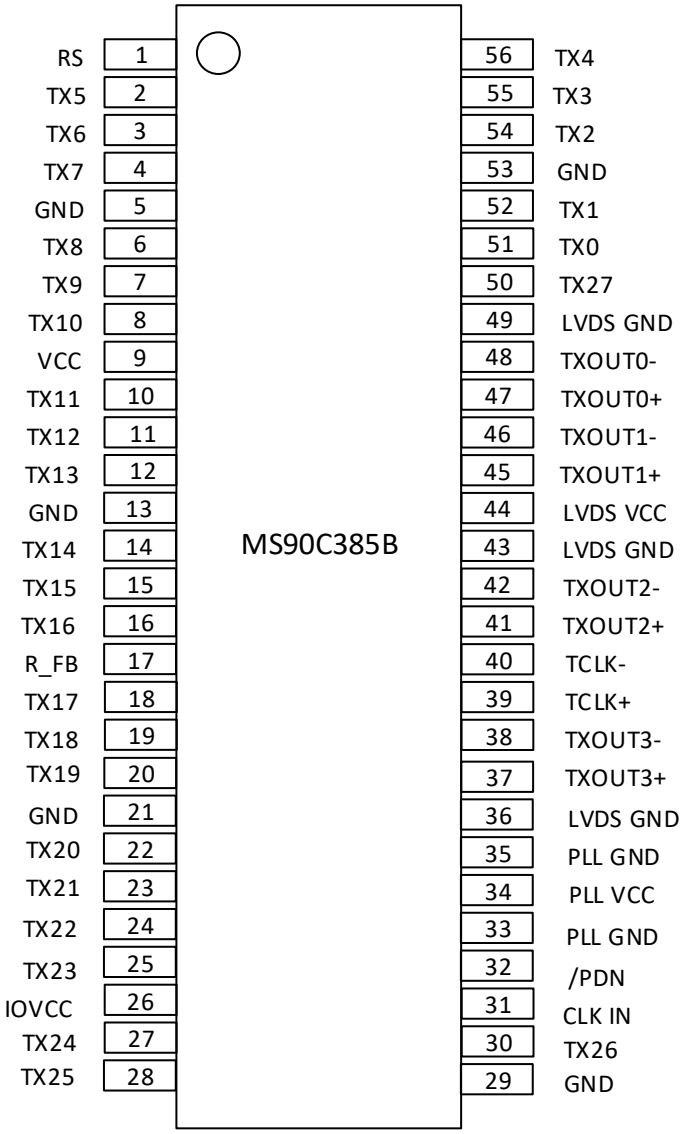
APPLICATIONS

- Monitor Camera
- Desktop/Laptop
- Printer

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS90C385B	TSSOP56	MS90C385B

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
47, 48	TXOUT0+, TXOUT0-	LVDS O	LVDS Differential Data Output
45, 46	TXOUT1+, TXOUT1-	LVDS O	
41, 42	TXOUT2+, TXOUT2-	LVDS O	
37, 38	TXOUT3+, TXOUT3-	LVDS O	
39, 40	TCLK+, TCLK-	LVDS O	LVDS Differential Clock Output
51, 52, 54, 55, 56, 2, 3	TX0~TX6	I	TTL Level Data Input. Include: 8 RED,8 GREEN,8 BLUE, 4 control signals (HSYNC, VXYNC, DE)
4, 6, 7, 8, 10, 11, 12	TX7~TX13	I	
14, 15, 16, 18, 19, 20, 22	TX14~TX20	I	
23, 24, 25, 27, 28, 30, 50	TX21~TX27	I	
31	CLK IN	I	TTL Level Clock Input
32	/PDN	I	TTL Level Input. High: Normal Operation Low: Low Power Dissipation
17	R_FB	I	Select Valid Edge. High: Rising Edge Low: Falling Edge
1	RS	I	LVDS Swing Control (Normal RS=VCC, Small Swing RS=GND)
9	VCC	P	Power Supply for Input Level, 3.3V Typical Value
26	IOVCC	IO P	IO Power Supply, Compatible with 1.8V and 3.3V
5, 13, 21, 29, 53	GND	-	Ground for TTL Level Input
44	LVDS VCC	P	LVDS Power Supply, 3.3V Typical Value
36, 43, 49	LVDS GND	-	Ground for LVDS Output
34	PLL VCC	P	PLL Power Supply, 3.3V Typical Value
33, 35	PLL GND	-	PLL Ground

Note:

When the MS90C385B is used, during the power-up, CLK IN (PIN31) needs to be in high-level state to ensure better compatibility.

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Condition	Ratings	Unit
Power Supply	VCC		-0.3 ~ 4	V
CMOS/TTL Input Voltage			-0.3 ~ (VCC+0.3)	V
CMOS/TTL Output Voltage			-0.3 ~ (VCC+0.3)	V
LVDS Driver Output Voltage			-0.3 ~ (VCC+0.3)	V
Operating Temperature	T		-40 ~ 100	°C
Maximum Power Dissipation (25°C)			1.4	W
Junction Temperature	T_J		-55 ~ 150	°C
Storage Temperature	T_{STG}		-65 ~ 150	°C
Lead Temperature (no plumbum)	T_{PEAK}		260	°C
Duration Time for Lead Temperature at T_{PEAK} (no plumbum)	T_P		10	s

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all power supplies are 3.3V±10%, V_A=25°C.

Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input High Voltage	V_{IH}		1.5		V_{CC}	V
Input low Voltage	V_{IL}		GND		0.8	V
Input High Current	I_{IH}	$V_{IN}=V_{CC}$		2.5	±10	μA
Input Low Current	I_{IL}	$V_{IN}=0$		0.5	±5	μA
Low Power-dissipation Current	I_{PD}	R_FB=V_{CC},$V_{IH}=V_{CC}$			10	μA

Switch Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Clock Cycle	t_C		6.90		50	ns
Delay	t_0	TxCLK Output Rising Edge to First Valid Data Output Time		0		ns
	t_1	TxCLK Output Rising Edge to Second Valid Data Output Time		1/7xt_C		ns
	t_2	TxCLK Output Rising Edge to Third Valid Data Output Time		2/7xt_C		ns
	t_3	TxCLK Output Rising Edge to Fourth Valid Data Output Time		3/7xt_C		ns
	t_4	TxCLK Output Rising Edge to Fifth Valid Data Output Time		4/7xt_C		ns
	t_5	TxCLK Output Rising Edge to Sixth Valid Data Output Time		5/7xt_C		ns
	t_6	TxCLK Output Rising Edge to Seventh Valid Data Output Time		6/7xt_C		ns
Output Clock Cycle		t_C=10ns		t_C		ns
Output Clock Adjacent Jitter		t_C=10ns		±30		ps
		t_C=7.2ns		±40		ps
Input Clock High-level Pulse Width		t_C=20ns		4/7xt_C		ns
Conversion Time for Differential Output Voltage	t_R	t_C=20ns		0.6		ns
	t_F	t_C=20ns		0.6		ns
Enable Time from PDN Rising Edge to Phase-lock	t_{EN}	f_{CLK}=135MHz		4		μs
PDN Falling Edge to Output High-impedance	t_{DIS}	f_{CLK}=135MHz		12		μs

DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Differential Output Voltage (RS=VCC)	V_{OD}	RL=100Ω	250	345	450	mV
Differential Output Voltage (RS=GND)			100	200	300	
Variation in Differential Output Voltage	ΔV_{OD}				35	mV
Common-mode Voltage (RS=VCC)	V_{OC}		1.125	1.19	1.375	V
Common-mode Voltage (RS=GND)			1.08	1.11	1.32	
Variation in Common-mode Output Voltage	ΔV_{OC}				40	mV
Peak-to-Peak for Common-mode Output Voltage	ΔV_{OCPP}	RL=100Ω, RS=GND			25	mV
Tri-state Output Current	I_{OZ}	PDN=0V, VOUT=0 or VCC			±10	μA
Short-circuit Output Current	I_{OS}	V_{OY}=0V		3.8	8	mA
		V_{OD}=0V		3.3	10	mA
High-impedance Output Current	I_{OZ}	V_O=0~VCC		8	±20	μA
Pull-down Resistance on Input Pin	R_{PDN}	All input pins		1200		kΩ
Quiescent Current	I_Q	All inputs are connected to GND, PDN=V_{IL}		200	300	μA

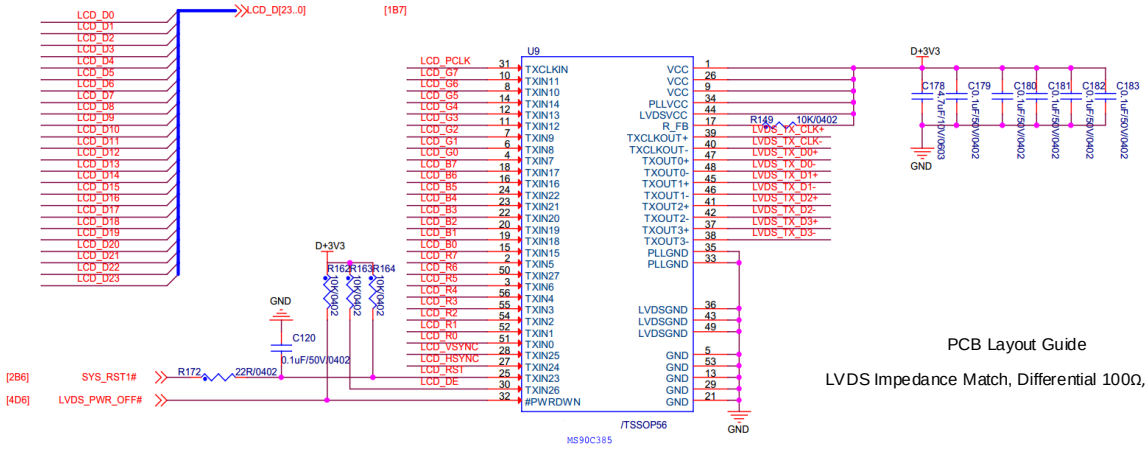
Power Supply Current

Parameter	Symbol	Condition	Typ	Max	Unit
Supply Current	I_{CC}	I(VCC)+I(PLLVCC)+I(LVDSVCC), PDN=V_{IH}, RL=100Ω, RS=VCC, green-level figure data, four channels data outputs+one channel clock output, VCC=3.3V, f_{CLK}=75MHz	41		mA
		I(VCC),PDN=V_{IH}, RL=100Ω, RS=VCC, green-level figure data, four channels data outputs+one channel clock output, VCC=3.3V, f_{CLK}=75MHz	18[1]		mA
		I(VCC)+I(PLLVCC)+I(LVDSVCC), PDN=V_{IH}, RL=100Ω, RS=VCC, 50% conversion density data, four channels data outputs+one channel clock output, VCC=3.3V, f_{CLK}=75MHz	35		mA
		I(VCC), PDN=V_{IH}, RL=100Ω, RS=VCC, 50% conversion density data, four channels data outputs+one channel clock output, VCC=3.3V, f_{CLK}=75MHz	17.5[1]		mA
		I(VCC)+I(PLLVCC)+I(LVDSVCC), PDN=V_{IH}, RL=100Ω, RS=VCC, 100% conversion density data (worst condition), four channels data outputs+one channel clock output, VCC=3.6V, f_{CLK}=75MHz	230		mA

Parameter	Symbol	Condition	Typ	Max	Unit
Supply Current	I_{CC}	I(VCC), PDN=V_{IH}, RL=100Ω, RS=VCC, 100% conversion density data (worst condition), four channels data outputs+one channel clock output,VCC=3.6V, f_{CLK}=75MHz	19[1]		mA
		I(VCC)+I(PLLVCC)+I(LVDSVCC), PDN=V_{IH}, RL=100Ω, RS=VCC, 100% conversion density data (worst condition), four channels data outputs+one channel clock output, VCC=3.6V, f_{CLK}=100MHz	248		mA
		I(VCC), PDN=V_{IH}, RL=100Ω, RS=VCC, 100% conversion density data (worst condition), four channels data outputs+one channel clock output, VCC=3.6V, f_{CLK}=100MHz	33[1]		mA
		I(VCC)+I(PLLVCC)+I(LVDSVCC), PDN=V_{IH}, RL=100Ω, RS=VCC, 100% conversion density data (worst condition), four channels data outputs+one channel clock output, VCC=3.6V, f_{CLK}=135MHz	315		mA
		I(VCC), PDN=V_{IH} , RL=100Ω, RS=VCC, 100% conversion density data (worst condition),four channels data outputs+one channel clock output, VCC=3.6V, f_{CLK}=135MHz	36[1]		mA

Note 1: Test VCC current, not IOVCC current.

TYPICAL APPLICATION DIAGRAM

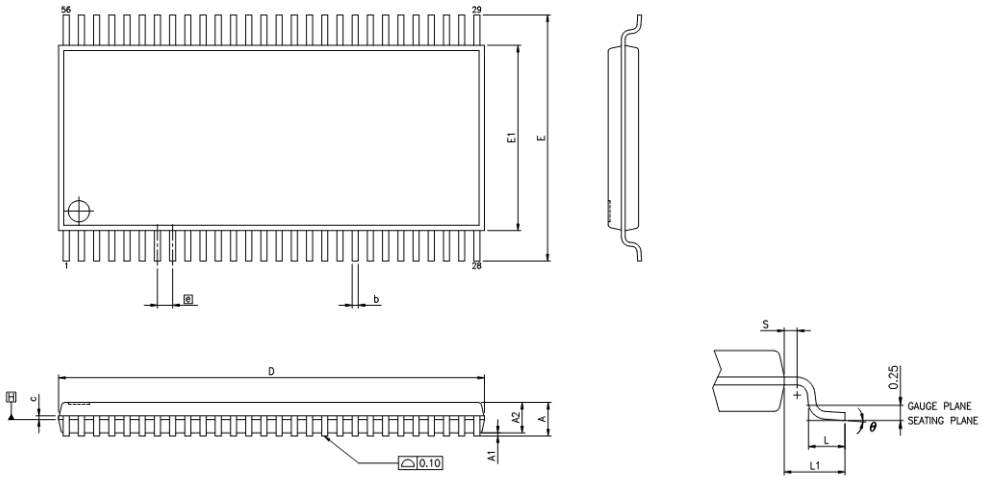


PCB Layout Guide

LVDS Impedance Match, Differential 100Ω, Error 10

PACKAGE OUTLINE DIMENSIONS

TSSOP56



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.17	-	0.27
c	0.09	-	0.20
D	13.90	14.00	14.10
E1	6.00	6.10	6.20
E	8.10BSC		
e	0.50BSC		
L1	1.00REF		
L	0.45	0.60	0.75
S	0.20	-	-
θ	0°	-	8°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name : MS90C385B

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS90C385B	TSSOP56	3000	1	3000	8	24000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

  Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

+86-571-89966911

Rm701, No.9 Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

http:// www.relmon.com