MS90C104

——+3.3V 175MHz 30bits COLOR LVDS Receiver

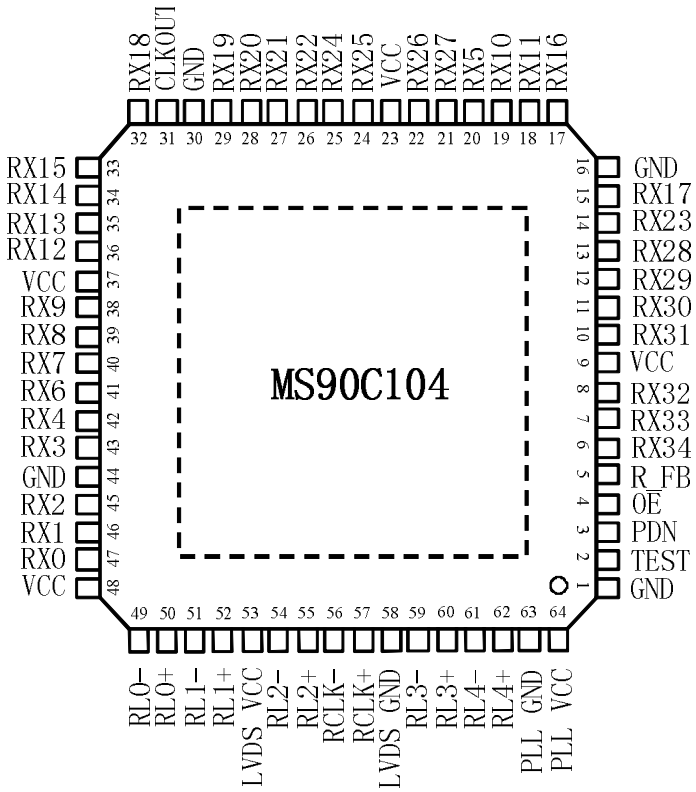
General Description

The MS90C104 receiver is designed to support pixel data transmission between Host and Flat Panel Display from NTSC up to SXGA resolutions. The MS90C104 converts the LVDS data streams back into 35bits of CMOS/TTL data with the choice of the rising edge or falling edge clock for the convenience with a variety of LCD panel controllers. At a transmit clock frequency of 175Mhz, 30bits of GRB data and 5bits of timing and control data (HSYNC,VSYCN,DE,CNTL1,CNTL2) are transmitted at an effective rate of 1225Mbps per LVDS channel. Using a 175MHz clock, the data throughput is 765.6Mbytes/sec.

Features

- Clock range: 8-175MHz
- Narrow bus reduces cable size
- Single 3.3V supply
- Power-down Mode
- Supports VGA、SVGA、XGA、SXGA
- Up to 6.125Gbps throughput
- Up to 765.6Megabytes/sec bandwidth
- PLL requires no external components
- Compatible with TIA/EIA-644 LVDS standard
- TQFP64 Package

Pin Diagram

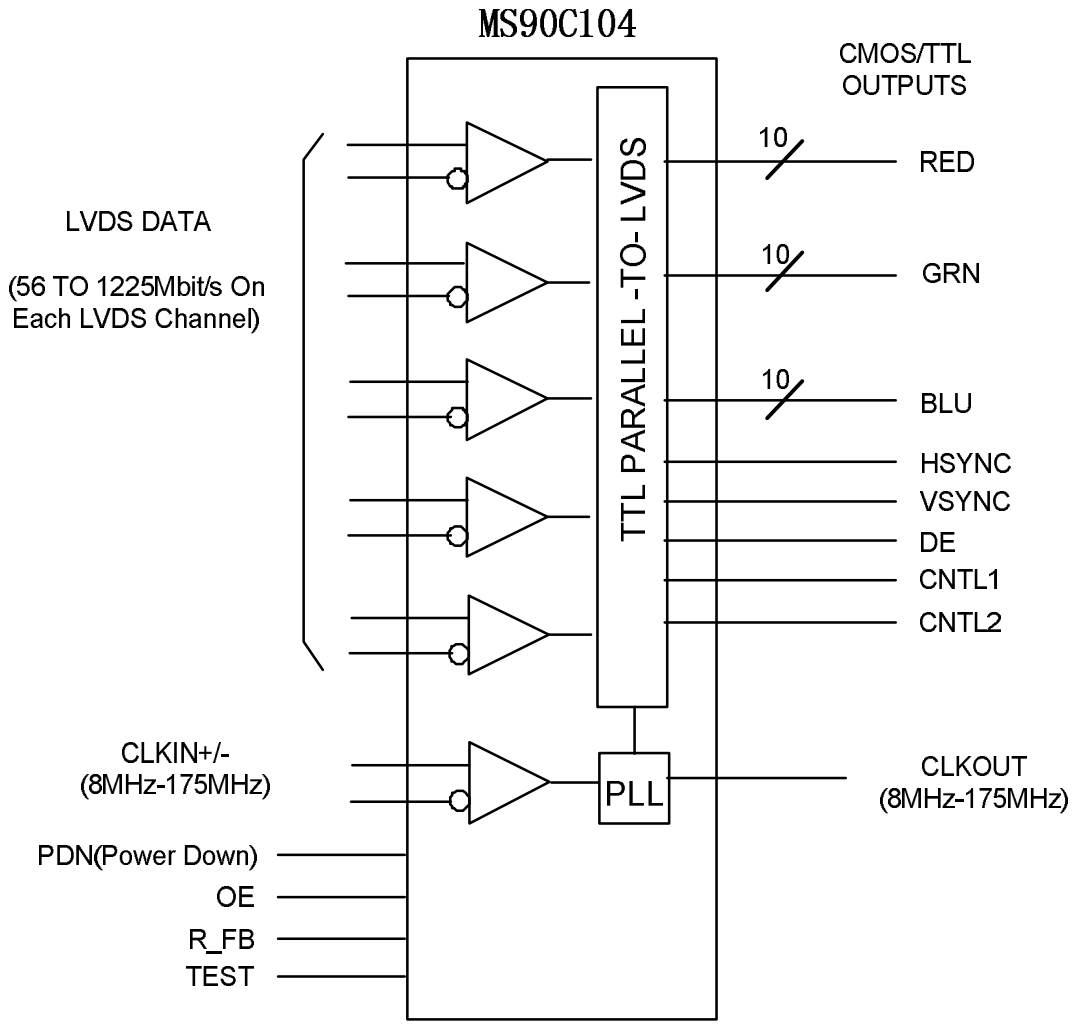


Pin Description

Pin Name	Pin No.	I/O	Description
RL0+, RL0-	49, 50	LVDS IN	LVDS differential data inputs
RL1+, RL1-	51, 52	LVDS IN	
RL2+, RL2-	54, 55	LVDS IN	
RL3+, RL3-	59, 60	LVDS IN	
RL4+, RL4-	61, 62	LVDS IN	
RCLK+, RCLK-	56, 57	LVDS IN	LVDS differential clock inputs
RxOUT0 ~ RxOUT6	47, 46, 45, 43, 42, 20, 41	OUT	TTL level data outputs. This includes: 10 RED, 10 GREEN, 10 BLUE, 5 control lines (HSYNC, VSYNC, DE,
RxOUT7 ~ RxOUT13	40, 39, 38, 19, 18, 36, 35	OUT	
RxOUT14 ~ RxOUT20	34, 33, 17, 15, 32, 29, 28	OUT	
RxOUT21 ~ RxOUT27	27, 26, 14, 25, 24, 22, 21	OUT	

RxOUT28 ~ RxOUT34	13, 12, 11, 10, 8, 7, 6	OUT	CNTL1, CNTL2)
CLKOUT	31	OUT	TTL level clock output.
PDN	25	IN	TTL level input. H: Normal operation L: Power down
OE	4	IN	TTL level input. H: Output Enable L: Output Disable
R_FB	5	IN	TTL level input. Out Clock Triggering Edge Select. H:Rising Edge L:Falling Edge
TEST	2	IN	Must be tied GND
Vcc	9, 23, 37, 48	Power	Power supply pins for TTL outputs.
GND	1, 16, 30, 44	Ground	Ground pins for TTL outputs.
LVDS Vcc	53	Power	Power supply pins for LVDS inputs.
LVDS GND	58	Ground	Ground pins for LVDS inputs.
PLL Vcc	64	Power	Power supply for PLL.
PLL GND	63	Ground	Ground pins for PLL.

Block Diagram



Absolute Maximum Ratings

Supply Voltage（VCC）	-0.3V - 4.0V
CMOS/TTL Input Voltage	-0.3V - (VCC+0.3V)
CMOS/TTL Output Voltage	-0.3V - (VCC+0.3V)
LVDS Input Voltage	-0.3V - (VCC+0.3V)
Junction Temperature	+150℃
Storage Temperature	-65℃ - 150℃
Lead Temperature(Soldering,4 sec)	+260℃
Maximum Power Dissipation Capacity (25℃)	
MS90C104	1.4W

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -4mA (data) I_{OH} = -8mA (clock)	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 4mA (data) I_{OL} = 8mA (clock)		0.06	0.3	V
I_{IN}	Input Current	$0 \leqslant V_{IN} \leqslant V_{CC}$			±10	uA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V			−50	mA

DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{OC} = +1.2V			+100	mV
V_{TL}	Differential Input Low Threshold		−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V/0V, V_{CC} = 3.6V			±10	uA

SUPPLY CURRENT

Symbol	Parameter	Conditions	Typ	Max	Units
ICC_{RG}	Supply Current (16 Grayscale)	CL = 8pF, f = 90MHz, Vcc = 3.3V 16 Grayscale Pattern	60	71	mA
ICC_{RW}	Supply Current (Worst Case)	CL = 8pF, f = 90MHz, Vcc = 3.3V Worst Case Pattern	96	102	mA
ICC_{RP}	Supply Current (Power Down)	PDN=0V		10	uA

Switching Characteristics

Symbol	Parameter	Min	Typ	Max	Units
T_{RCP}	CLKOUT Period	11.1	T	125	ns
T_{RCH}	CLKOUT High Time		T/2		ns

T_{RCL}	CLKOUT Low Time			T/2		ns
T_{RS}	TTL Data Setup to CLKOUT		5.0			ns
T_{RH}	TTL Data Hold from CLKOUT		1.0			ns
T_{TLH}	TTL Low to High Transition Time			2	3	ns
T_{THL}	TTL High to Low Transition Time			2	3	ns
T_{RCD}	RCLK to CLKOUT Delay			7.0		ns
T_{RDP5}	Position 0	175MHz	-0.4	0	+0.4	ns
T_{RDP6}	Position 1		T/7-0.4	T/7	T/7+0.4	ns
T_{RDP0}	Position 2		2T/7-0.4	2T/7	2T/7+0.4	ns
T_{RDP1}	Position 3		3T/7-0.4	3T/7	3T/7+0.4	ns
T_{RDP2}	Position 4		4T/7-0.4	4T/7	4T/7+0.4	ns
T_{RDP3}	Position 5		5T/7-0.4	5T/7	5T/7+0.4	ns
T_{RDP4}	Position 6		6T/7-0.4	6T/7	6T/7+0.4	ns
T_{TPLLS}	PLL Set		-	-	10	ms

AC Timing Diagram

FIGURE 1. Test Pattern “Worst Case Pattern”

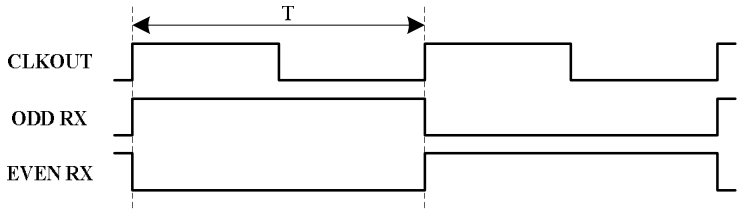


FIGURE 2. Test Pattern “16 Grayscale Test Pattern”

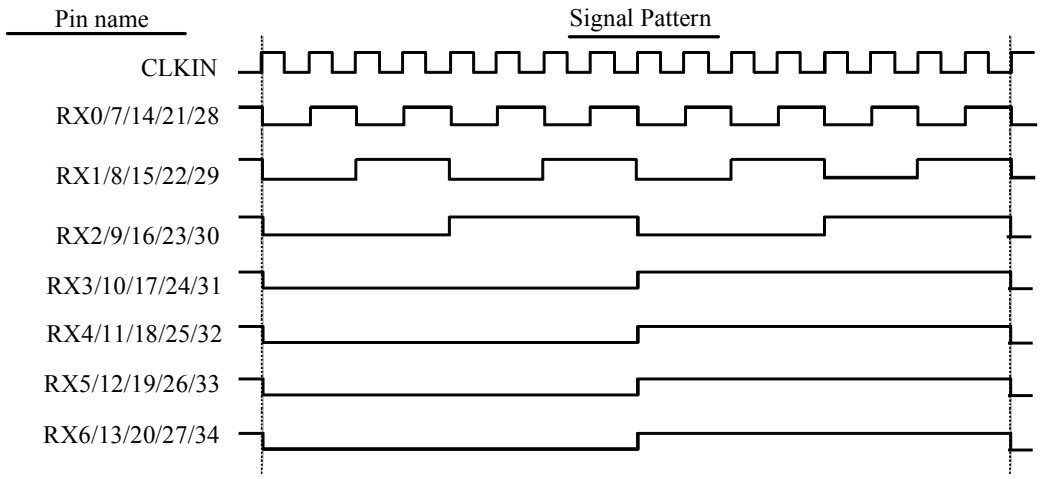


FIGURE 3. TTL Output

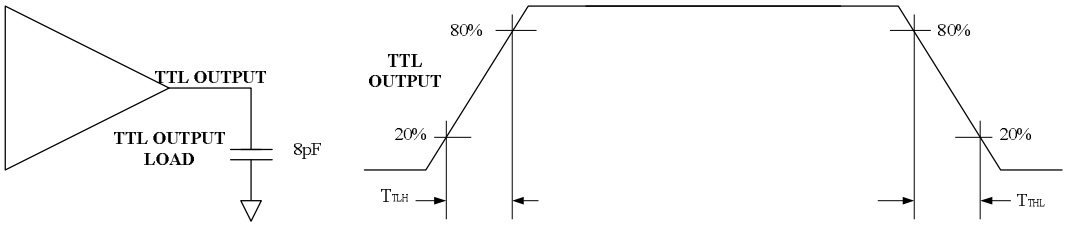


FIGURE 4.PLL Set Time

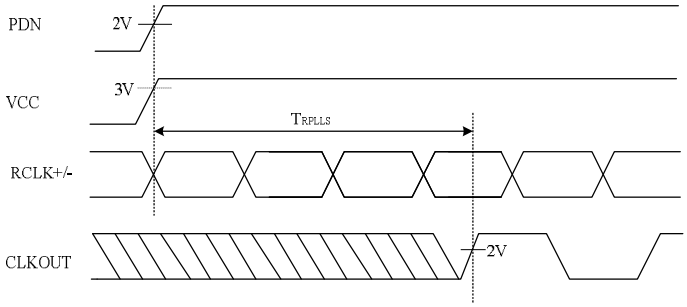
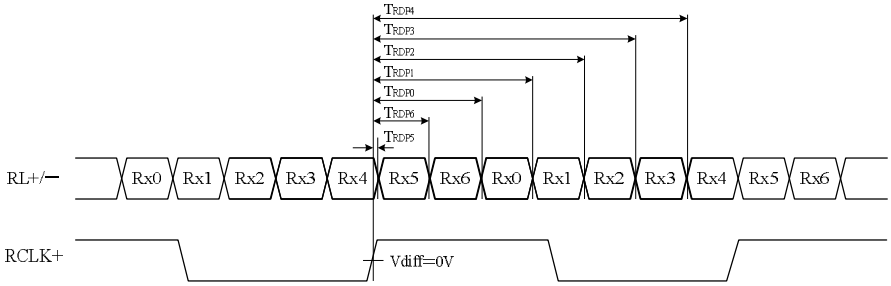


FIGURE 5.Receiver Device Operation



Vdiff= (RxIN+) - (RxIN-),…… (RxCLKIN+) - (RxCLKIN-)

FIGURE 6.LVDS Inputs Mapped Parallel TTL Data Outputs

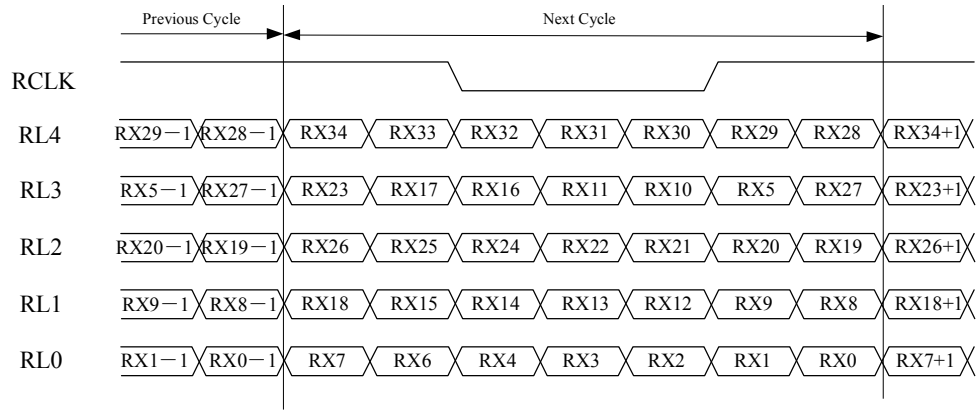
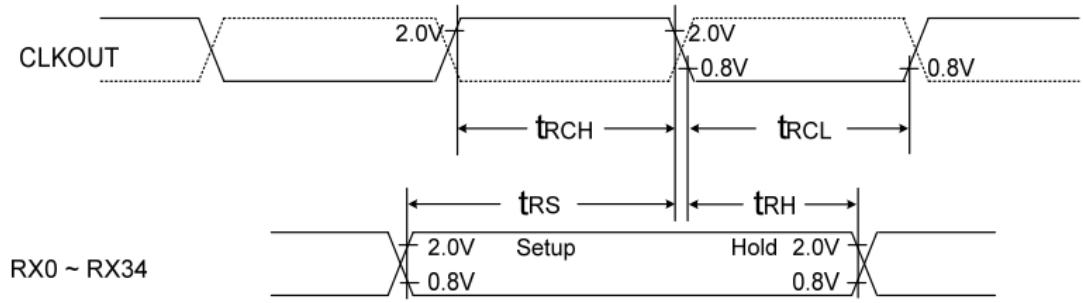
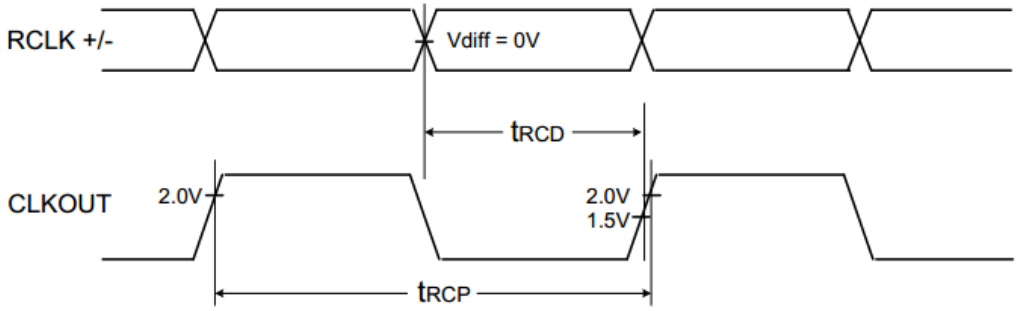


FIGURE 7. Setup/Hold and High/Low Times



NOTE: CLKOUT: R_FB=0 Solid line; R_FB=1 Dotted line.

FIGURE 8. RCLK to CLKOUT Delay



Package

64 Pin TQFP Package, JEDEC [Unit : millimeters]