192kHz Digital Audio Receiver/Converter（D/A）

Product Description

MS8412 is a monolithic CMOS device that receives and decodes one of four stereo pairs of digital audio data according to the IEC60958,S/PDIF,EIAJ CP1201,or AES3 interface standards. MS8412 includes interpolation, multi-bit D/A conversion and output analog filtering. The MS8412 contains on-chip digital de-emphasis, operates from a single +3.3 V or +5 V power supply.These features are ideal for DVD players & recorders, digital televisions.

The MS8412 is available in a 28-pin SSOP package.

SSOP28

Features

- Complete EIAJ CP1201, IEC-60958, AES3, S/PDIF-Compatible Receiver
- +3.3 V or +5 V Power Supply
- 4:1 S/PDIF Input MUX
- I²C Interface
- 32 kHz to 192 kHz Sample Frequency Range
- Low-Jitter Clock Recovery
- Single-ended or differential input
- Multi-bit Delta-Sigma Modulator
- 24-bit Conversion
- 105 dB Dynamic Range
- -90 dB THD+N
- Low Clock-Jitter Sensitivity
- On-chip Digital De-emphasis

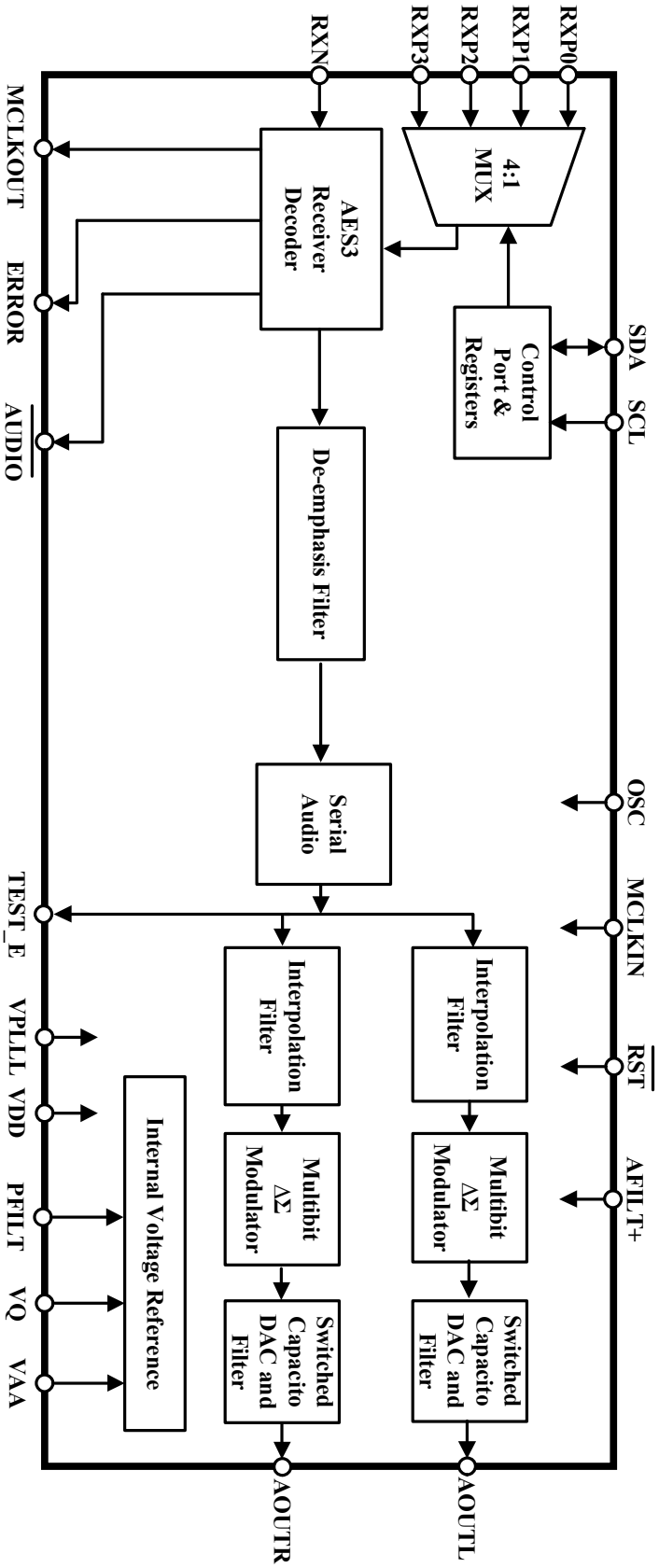
Applications

- A/V receivers
- CD-R,DVD receivers
- multimedia speakers
- digital mixing consoles
- effects processors
- set-top boxes
- computer
- automotive audio systems

Package/Ordering Information

Part Number	Package	Marking
MS8412	SSOP-28	MS8412

Block Diagram



1、CHARACTERISTICS AND SPECIFICATIONS

All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.

SPECIFIED OPERATING CONDITIONS

(AGND, GND = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	VAA VDD VPLL	3.2	3.3 or 5.0	5.25	V
Ambient Operating Temperature: Commercial Grade Automotive Grade	T_A	-10 -40	- -	+70 +85	℃

ABSOLUTE MAXIMUM RATINGS

(AGND, GND = 0 V; all voltages with respect to 0 V. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	VAA,VDD, VPLL	-	5.5	V
Input Current, Any Pin Except Supplies (Note 1)	I_{in}	-	±10	mA
Input Voltage	V_{in}	-0.3	（VDD）+0.3	V
Ambient Operating Temperature (power applied)	T_A	-55	125	℃
Storage Temperature	T_{stg}	-65	150	℃

Notes:

1. Transient currents of up to 100 mA will not cause SCR latch-up.

DC ELECTRICAL CHARACTERISTICS

(AGND = GND = 0 V; all voltages with respect to 0 V.)

Parameters		Symbol	Min	Typ	Max	Units
Power-Down Mode (Notes 2, 4)						
Supply Current in power-down	VAA	IAA	-	110	-	μA
	VDD	IDD	-	70	-	μA
	VPLL=3.3V	IPLL	-	10	-	μA
	VPLL=5.0V	IPLL	-	12	-	μA
Normal Operation (Notes 3, 4)						
Supply Current at 48 kHz frame rate	VAA	IAA	-	22	-	mA
	VDD	IDD	-	6.9	-	mA
	VPLL=3.3V	IPLL	-	3.8	-	mA
	VPLL=5.0V	IPLL	-	5.2	-	mA
Supply Current at 192 kHz frame rate	VAA	IA	-	27	-	mA
	VDD	IDD	-	23	-	mA
	VPLL=3.3V	IL	-	8.8	-	mA
	VPLL=5.0V	IL	-	12.8	-	mA

Notes:

2. Power-Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.

3. Normal operation is defined as $\overline{RST}$ = HI.

4. Assumes that no inputs are floating. It is recommended that all inputs be driven high or low at all times.

DIGITAL INPUT CHARACTERISTICS

(AGND = GND = 0 V; all voltages with respect to 0 V.)

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	I_{IN}	-	-	±0.5	μA
Differential Input Sensitivity, RXP[3:0] to RXN	V_{TH}	-	150	200	mVpp
Input Hysteresis	V_H	0.15	-	1.0	V

DIGITAL INTERFACE SPECIFICATIONS

(AGND = GND = 0 V; all voltages with respect to 0 V.)

Parameters	Symbol	Min	Max	Units
High-Level Output Voltage(I_{OH}=-3.2mA)	V_{OH}	(VDD)-1.0	-	V
Low-Level Output Voltage(I_{OL}=3.2mA)	V_{OL}	-	0.5	V
High-Level Input Voltage, except RXP[3:0], RXN	V_{IH}	2.0	(VDD)+0.3	V
Low-Level Input Voltage, except RXP[3:0], RXN	V_{IL}	-0.3	0.8	V

DAC ANALOG CHARACTERISTICS 1

(T_A = 25°C， Full-Scale Output Sine Wave, 997 Hz, Fs= 48/96/192 kHz; Test load R_L = 3 kΩ, C_L = 10 pF, Measurement Bandwidth 10 Hz to 20 kHz.)

Parameters			5V			3.3V			Unit
			Min	Typ	Max	Min	Typ	Max	
Dynamic Range	18 to 24 bit	A-weighted	99	105		97	103		dB
		unweighted	96	102		94	100		dB
	16bit	A-weighted	90	96		90	96		dB
		unweighted	87	93		87	93		dB
Total Harmonic Distortion + Noise	18 to 24 bit	0dB		-90	-85		-90	-85	dB
		-20dB		-82	-76		-80	-74	dB
		-60dB		-42	-36		-40	-34	dB
	16bit	0dB		-90	-84		-90	-84	dB
		-20dB		-73	-67		-73	-67	dB
		-60dB		-33	-27		-33	-27	dB
Dynamic Range	18 to 24 bit	A-weighted	95	105		93	103		dB
		unweighted	92	102		90	100		dB
	16bit	A-weighted	86	96		86	96		dB
		unweighted	83	93		83	93		dB
Total Harmonic Distortion + Noise	18 to 24 bit	0dB		-90	-82		-90	-82	dB
		-20dB		-82	-72		-80	-70	dB
		-60dB		-42	-32		-40	-30	dB
	16bit	0dB		-90	-82		-90	-82	dB
		-20dB		-73	-63		-73	-63	dB
		-60dB		-33	-23		-33	-23	dB

DAC ANALOG CHARACTERISTICS 2

(T_A = 25°C， Full-Scale Output Sine Wave, 997 Hz, Fs= 48/96/192 kHz; Test load R_L = 3 kΩ, C_L = 10 pF, Measurement Bandwidth 10 Hz to 20 kHz.)

Parameter	Symbol	Min	Typ	Max	Unit
Interchannel Isolation (1 kHz)		-	100		dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	0.25	dB
Gain Drift		-	100	-	ppm/°C
Analog Output					
Full Scale Output Voltage			0.65•VAA		Vpp
Quiescent Voltage	VQ		0.5•VAA		VDC
Max DC Current draw from an AOUT pin	IOUTmax		10		uA
Max Current draw from VQ	IQmax		100		uA
Max AC-Load Resistance	RL		3		kΩ
Max Load Capacitance	CL		100		pF
Output Impedance	Zout		100		Ω

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode						
Passband	to -0.1 dB corner		0	-	.35	Fs
	to -3 dB corner		0		.4992	Fs
Frequency Response 10 Hz to 20 kHz			-0.175		+.01	dB
StopBand			0.5465			Fs
StopBand Attenuation			50			dB
Group Delay		T_{gd}		10/fs		s
De-emphasis Error	Fs＝32KHZ				+1.5/+0	
	Fs＝44.1KHZ				+.05/-.25	
	Fs＝48KHZ				-.2/-.4	
Double-Speed Mode						
Passband	to -0.1 dB corner		0	.	.22	Fs
	to -3 dB corner		0		.501	Fs
Frequency Response 10 Hz to 20 kHz			-0.15		+.015	dB
StopBand			0.5770			Fs
StopBand Attenuation			55			dB
Group Delay		T_{gd}		5/fs		s

Quad-Speed Mode						
Passband	to -0.1 dB corner		0	.	.11	Fs
	to -3 dB corner		0		.469	Fs
Frequency Response 10 Hz to 20 kHz			-0.12		+0	dB
StopBand			07			Fs
StopBand Attenuation			51			dB
Group Delay		T_{gd}		2.5/fs		s

SWITCHING CHARACTERISTICS

(Inputs: Logic 0 = 0 V, Logic 1 = VDD; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{RST}$ Pin Low Pulse Width		200	-	-	μs
PLL Clock Recovery Sample Rate Range		30	-	200	kHz
MCLKOUT Output Jitter （Note 5）		-	200	-	ps RMS
MCLKOUT Output Duty-Cycle （Note 6）		45	50	55	%
（Note 7）		50	55	65	%

Notes:

5. Typical RMS cycle-to-cycle jitter.

6. Duty cycle when clock is recovered from bi-phase encoded input.

7. Duty cycle when MCLKIN is switched over for output on MCLKOUT.

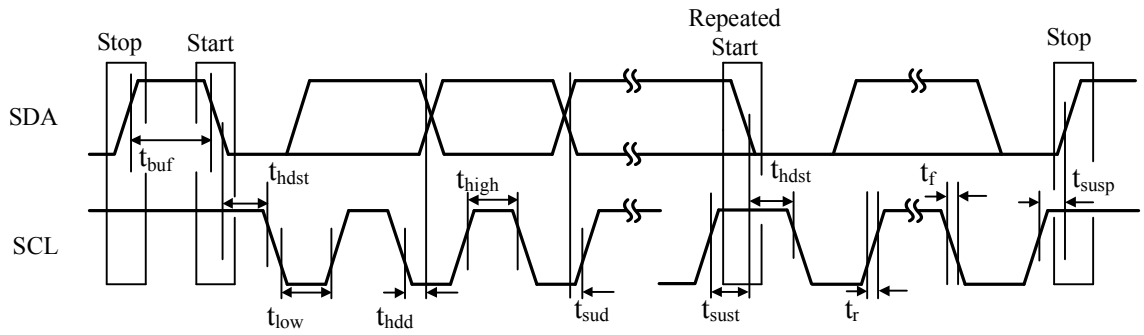
SWITCHING CHARACTERISTICS - CONTROL PORT- I²C FORMAT

(Inputs: Logic 0 = 0 V, Logic 1 = VDD; C = 20 pF)

Parameter	Symbol	Min	Typ	Units
SCL Clock Frequency	f_{scl}	-	100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7	-	μs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	μs
Clock Low time	t_{low}	4.7	-	μs
Clock High Time	t_{high}	4.0	-	μs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	μs
SDA Hold Time from SCL Falling （Note8）	t_{hdd}	10	-	ns
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_r	-	1000	ns
Fall Time SCL and SDA	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	μs

Notes:

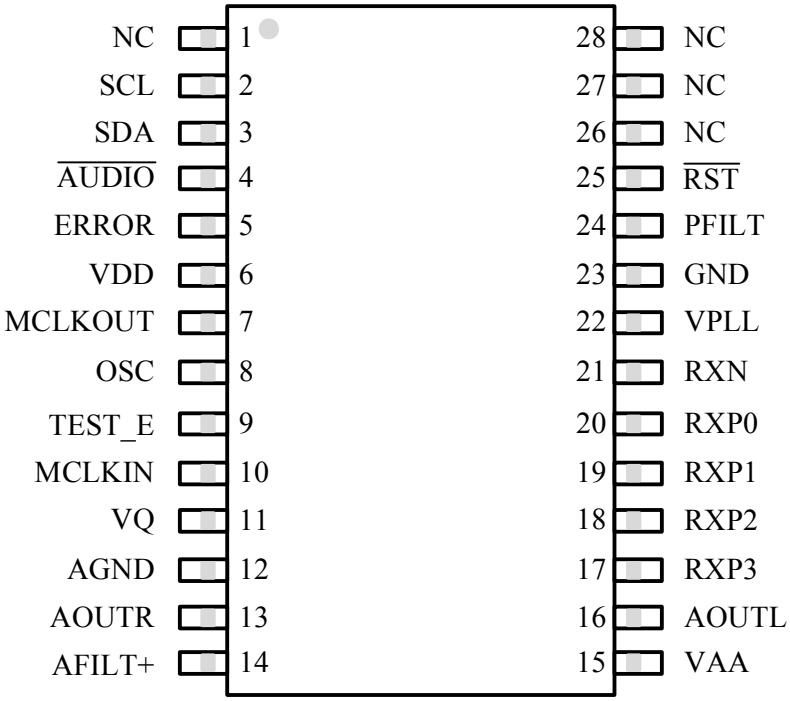
8. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.


Stop
Start
Repeated
Start
Stop
SDA
SCL
t_{buf}
t_{hdst}
t_{high}
t_{hdst}
t_f
t_{susp}
t_{low}
t_{hdd}
t_{sud}
t_{sust}
t_r

I^2C Timing

2、PIN DESCRIPTION

2.1 MS8412 Pin Description



Pin Name	Pin #	Type	Pin description
NC	1		Float
SCL	2	I	Control Port Clock (Input) - Serial control interface clock and is used to clock control data bits into and out of the MS8412. See the “Control Port Description” .
SDA	3	I/O	Serial Control Data I/O (I^2C) - SDA is the control I/O data line. SDA is open drain and requires an external pull-up resistor to VDD. See the “Control Port Description”.
$\overline{\text{AUDIO}}$	4	O	When low, a valid linear PCM audio stream is indicated.
ERROR	5	O	Receiver error indicator. If the received S/PDIF data are unstable or no S/PDIF input, this pin will output “1”.
VDD	6	P	Digital core power supply.
MCLKOUT	7	O	S/PDIF recovered master clock output from the PLL, must be connected with PIN10.
OSC	8	O	Connect with crystal oscillator, when PLL is unlocked, MCLKOUT willfollow this clock.
TEST_E	9	O	Serial audio data output monitor pin.This pin must be pulled up to VDD through a 47 kΩ resistor.
MCLKIN	10	I	Internal DAC master clock input port, must be connected with PIN7.
VQ	11	O	Filter connection for internal quiescent voltage.
AGND	12	G	Ground

AOUTR	13	O	Analog output: right channel output port
AFILT+	14	O	Positive reference voltage for the internal sampling circuits.
VAA	15	P	Analog power supply.
AOUTL	16	O	Analog output: left channel output port
RXP3	17	I	Single-ended or differential receiver inputs carrying S/PDIF encoded digital data.The RXP[3:0] inputs comprise the 4:1 S/PDIF Input Multiplexer. Unused multiplexer inputs should be left floating or tied to AGND.
RXP2	18		
RXP1	19		
RXP0	20		
RXN	21	I	Single-ended or differential receiver input carrying S/PDIF encoded digital data. In single-ended operation this should be AC coupled to ground through a capacitor.
VPLL	22	P	Internal PLL power supply, +3.3 V. This power supply must be guaranteed low noise, insure internal PLL is stable.
GND	23	G	Internal PLL ground
PFILT	24	O	PLL Loop Filter output. An RC network should be connected between this pin and pin 23.
$\overline{\text{RST}}$	25	I	When $\overline{\text{RST}}$ is low, the MS8412 enters a low power mode and all internal states are reset. On initial power up, $\overline{\text{RST}}$ must be held low until the power supply is stable, and all input clocks are stable in frequency and phase.
NC	26		Float
NC	27		
NC	28		

3、TYPICAL CONNECTION DIAGRAMS

The typical input structure and the recommended input circuit are detailed in “S/PDIF Receiver” and “AES3 Receiver External Components”.(If necessary, can provide the relevant accessories.)

To get the best jitter performance, the grand of filter is directly connected to the pin AGND. See “Table 2. External PLL Component Values”.

4、APPLICATIONS

4.1 Reset, Power-Down and Start-Up

When $\overline{RST}$ is low, the MS8412 enters a low power mode and all internal states are reset, including the control port and registers, and the outputs are muted. After the PLL has settled, the serial audio outputs will be enabled.

4.2 Power Supply, Grounding, and PCB Layout

For most applications, the MS8412 can be operated from a single +3.3 V supply, following normal supply decoupling practices. For applications where the recovered input clock, output on the MCLKOUT pin, is required to be low jitter, then use a separate, quiet, analog +3.3 V supply for VAA, decoupled to AGND. Make certain that no digital traces are routed near VAA, AGND, or FILT as noise may couple and degrade performance. These pins should be well isolated from switching signals and other noise sources.

VDD sets the level for the digital inputs and outputs, as well as the AES/SPDIF receiver inputs.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be mounted on the same side of the board as the MS8412 to minimize inductance effects, and all decoupling capacitors should be as close to the MS8412 as possible.

5、GENERAL DESCRIPTION

The MS8412 is a monolithic CMOS device that receives and decodes audio data according to the AES3, IEC60958, S/PDIF, and EIAJ CP1201 interface standards. The MS8412 accepts data at standard audio sample rates including 48, 44.1 and 32 kHz in SSM, 96, 88.2 and 64 kHz in DSM, and 192, 176.4 and 128 kHz in QSM.

The MS8412 provides an 4:1 multiplexer to select between four inputs for decoding. Input data can be either differential or single-ended.

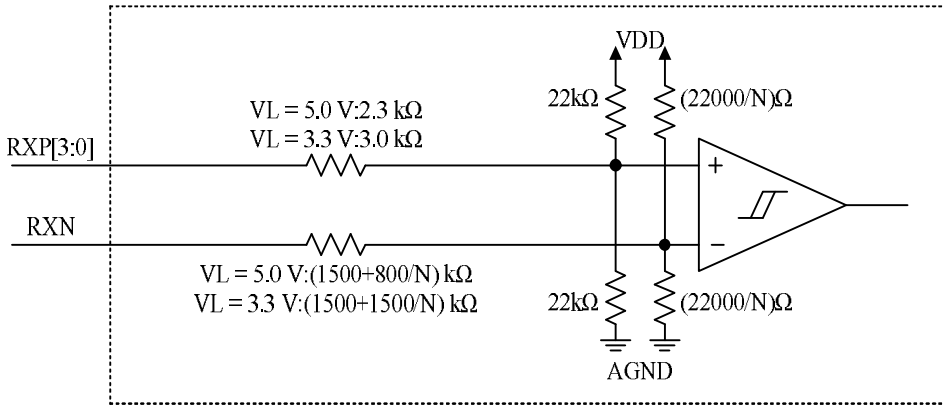
5.1 AES3 and S/PDIF Standards Documents

This document assumes that the user is familiar with the AES3 and S/PDIF data formats. It is advisable to have current copies of the AES3, IEC60958, and IEC61937 specifications on hand for easy reference.

The latest AES3 standard is available from the Audio Engineering Society or ANSI at www.aes.org or at www.ansi.org. Obtain a copy of the latest IEC60958/61937 standard from ANSI or from the International Electrotechnical Commission at www.iec.ch. The latest EIAJ CP-1201 standard is available from the Japanese Electronics Bureau.

5.2 AES3/SPDIF Receiver

The MS8412 includes an AES3/SPDIF digital audio receiver. The receiver accepts and decodes bi-phase encoded audio and digital data according to the AES3, IEC60958 (S/PDIF), and EIAJ CP-1201 interface standards. The receiver consists of an analog differential input stage, driven through analog input pins RXP0 to RXP3 and a common RXN, A PLL based clock recovery circuit, and a decoder which separates the audio data from the channel status and user data. External components are used to terminate the incoming data cables and isolate the MS8412. Figure shows the input structure of the receiver.



If RXP[3:0] is selected by either the receiver MUX MUX,N=1.
If RXP[3:0] is not selected at all,N=0(i.e. high impedance).

The MS8412 employs a 4:1 S/PDIF input multiplexer to accommodate up to four channels of input digital audio data. Digital audio data may be single-ended or differential. Differential inputs utilize RXP[3:0] and a shared RXN. Single ended signals are

accommodated by using the RXP[3:0] inputs and AC coupling RXN to ground.
All active inputs to the MS8412 4:1 input multiplexer should be coupled through a capacitor as these inputs are biased at VDD/2 when selected. These inputs are floating when not selected. Unused multiplexer inputs should be left floating or tied to AGND. The recommended capacitor value is 0.01 μF to 0.1 μF. The recommended dielectrics for the AC coupling capacitors are C0G or X7R.
The input voltage range for the input multiplexer is set by the I/O power supply pin, VDD. The input voltage of the RXP[3:0] and RXN pins is also set by the level of VDD. Input signals with voltage levels above VDD or below GND may degrade performance or damage the part.

5.2.1 Multiplexer

The multiplexer select line control is accessed through bits RXSEL[2:0] in control port register 04h. The multiplexer defaults to RXP0.

5.3 Clock Recovery and PLL Filter

Please see "PLL Filter" for a general description of the PLL, selection of recommended PLL filter components, and layout considerations.

5.4 Error

While decoding the incoming bi-phase encoded data stream, the MS8412 has the ability to identify various error conditions.
The user can view receiver error on the ERROR pin.
ERROR – The previous audio sample is held and passed to the serial audio output port if a parity, bi-phase, confidence or PLL lock error occurs during the current sample.

5.5 Non-Audio Detection

An AES3 data stream may be used to convey non-audio data, thus it is important to know whether the incoming AES3 data stream is digital audio or not. This information is typically conveyed in channel status bit 1, which is extracted automatically by the MS8412. However, certain non-audio sources, such as AC-3™ or MPEG encoders, may not adhere to this convention, and the bit may not be properly set. The MS8412 AES3 receiver can detect such non-audio data through the use of an autodetect module.
If the AES3 stream contains sync codes in the proper format for IEC61937 or DTS® data transmission, an internal auto detect signal will be asserted. If the sync codes no longer appear after a certain amount of time, autodetection will time-out and auto detect will be de-asserted until another format is detected.
$\overline{AUDIO}$ is output on pin 1. If non-audio data is detected, the data is still processed exactly as if it were normal audio. The exception is the use of de-emphasis auto-select feature which will bypass the de-emphasis filter if the input stream is detected to be non-audio. It is up to the user to mute the outputs as required.

5.6 AES3 Receiver External Components

The MS8412 AES3 receiver is designed to accept both the professional and consumer

interfaces. The digital audio specifications for professional use call for a balanced receiver, using XLR connectors, with 110 Ω ± 20% impedance. The XLR connector on the receiver should have female pins with a male shell. Since the receiver has a very high input impedance, a 110 Ω resistor should be placed across the receiver terminals to match the line impedance, as shown in Figures 1 and 2. Although transformers are not required by the AES specification, they are strongly recommended.

If some isolation is desired without the use of transformers, a 0.01 µF capacitor should be placed in series with each input pin (RXP[3:0] and RXN) as shown in Figure 2. However, if a transformer is not used, high frequency energy could be coupled into the receiver, causing degradation in analog performance.

Figures 1 and 2 show an optional (recommended) DC blocking capacitor (0.1 µF to 0.47 µF) in series with the cable input. This improves the robustness of the receiver, preventing the saturation of the transformer, or any DC current flow, if a DC voltage is present on the cable.

In the case of the consumer interface, the standards call for an unbalanced circuit having a receiver impedance of 75 Ω ±5%. The connector for the consumer interface is an RCA phono socket. The receiver circuit for the consumer interface is shown in Figure 3. An implementation of the Input S/PDIF Multiplexer using the consumer interface is shown in Figure 4.

The circuit shown in Figure 5 may be used when external RS422 receivers, optical receivers or other TTL/CMOS logic outputs drive the MS8412 receiver section.

In the configuration of systems, it is important to avoid ground loops and DC current flowing down the shield of the cable that could result when boxes with different ground potentials are connected. Generally, it is good practice to ground the shield to the chassis of the transmitting unit, and connect the shield through a capacitor to chassis ground at the receiver. However, in some cases it is advantageous to have the ground of two boxes held to the same potential, and the cable shield might be depended upon to make that electrical connection. Generally, it is a good idea to provide the option of grounding or capacitively coupling the shield to the chassis.

5.6.1 Isolating Transformer Requirements

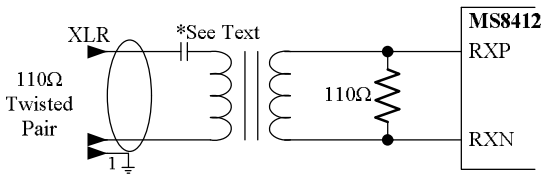


Figure 1. Professional Input Circuit

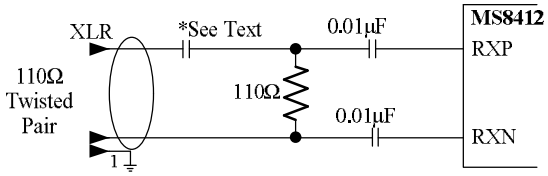


Figure 2. Transformerless Professional Input Circuit

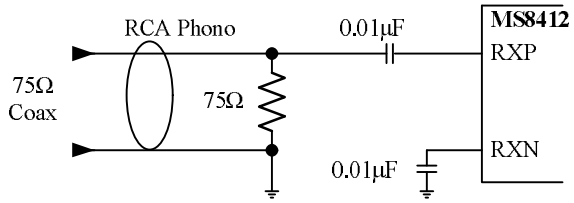


Figure 3. Consumer Input Circuit

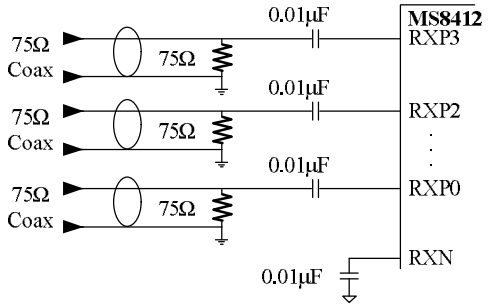


Figure 4. S/PDIF MUX Input Circuit

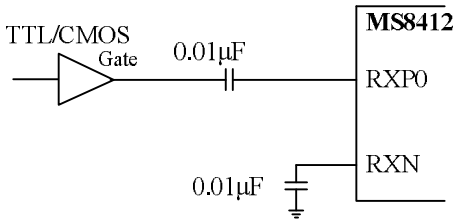


Figure 5. TTL/CMOS Input Circuit

5.7 PLL Filter

Board layout and capacitor choice affect each other and determine the performance of the PLL. Figure 6 contains a suggested layout for the PLL filter components and for bypassing the analog supply voltage. The 0.1 µF bypass capacitor is in a 1206 form factor. R_{FLT}, C_{FLT}, C_{RIP}, and the 1000 pF decoupling capacitor are in an 0805 form factor. The traces are on the top surface of the board with the IC so that there is no via inductance. The traces themselves are short to minimize the inductance in the filter path. The VAA and AGND traces extend back to their origin and are shown only in truncated form in the drawing.

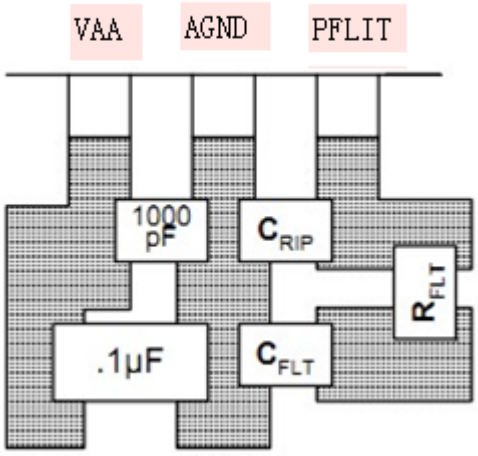


Figure 6. Recommended Layout Example

The external PLL component values are listed in Table 2.

Table 2. External PLL Component Values

Range (kHz)	R_{FLT}	C_{FLT}	C_{RIP}	Settling Time
32 - 192	3kΩ	22nF	1nF	4ms

5.8 Jitter Attenuation

Shown in Figure 7 is the jitter attenuation plot. The AES3 and IEC60958-4 specifications state a maximum of 2 dB jitter gain or peaking.

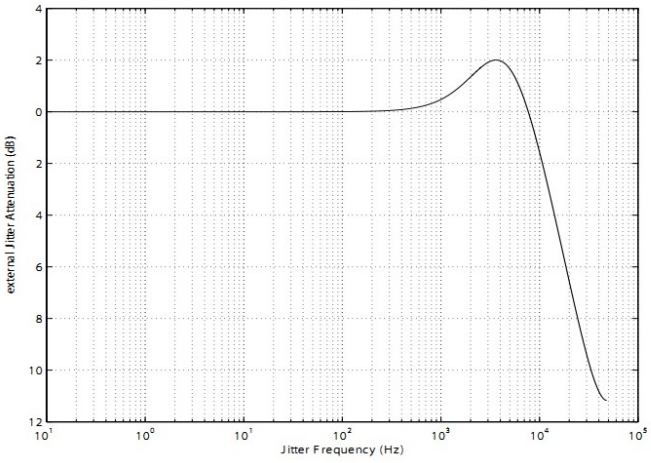


Figure 7. Jitter Attenuation Characteristics of PLL

5.9 De-Emphasis

The MS8412 includes on-chip digital de-emphasis. Figure 8 shows the de-emphasis curve for Fs equal to 44.1 kHz.

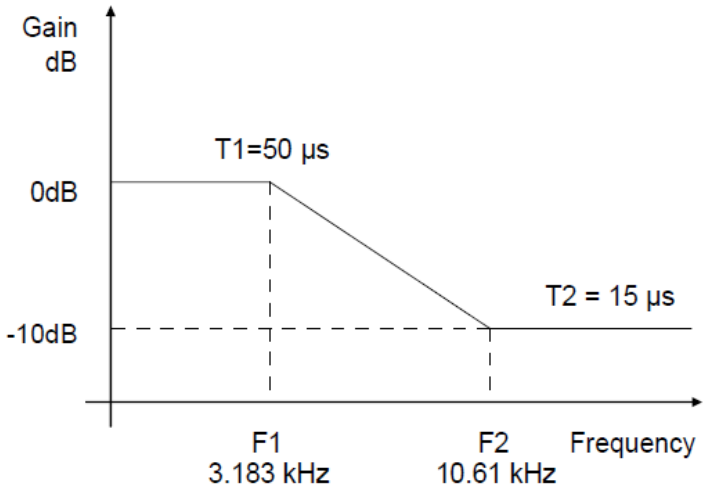


Figure 8. De-Emphasis Curve (Fs = 44.1kHz)

5.10 Analog Output Initialization and Power-Down

The MS8412 enters the Power-Down State upon initial power-up. The interpolation filters and delta-sigma modulators are reset, and the internal voltage reference, multi-bit digital-to-analog converters and switched-capacitor low-pass filters are powered down. The device will remain in the Power-down mode until MCLK is present. Power is then applied to the internal voltage reference. Finally, power is applied to the D/A converters and switched-capacitor filters, and the analog outputs will ramp to the quiescent voltage VQ.

5.10.1 Output Transient Control

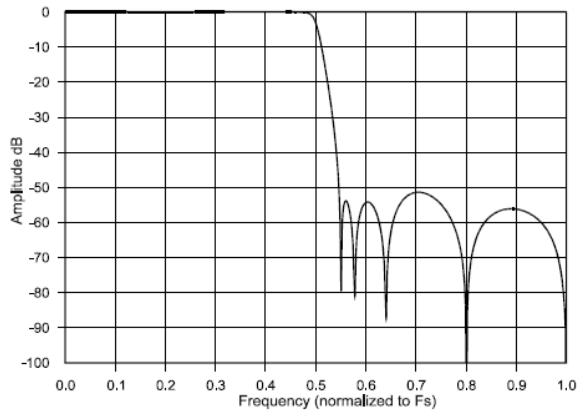
The MS8412 uses Popguard technology to minimize the effects of output transients during power-up and power-down.

(1) Power-Up: When the device is initially powered-up, the audio outputs, AOUTL and AOUTR, are clamped to VQ which is initially low. After MCLK is applied the outputs begin to ramp with VQ towards the nominal quiescent voltage. This ramp takes approximately 250 ms with a 3.3 µF cap connected to VQ (420 ms with a 10 µF connected to VQ) to complete.

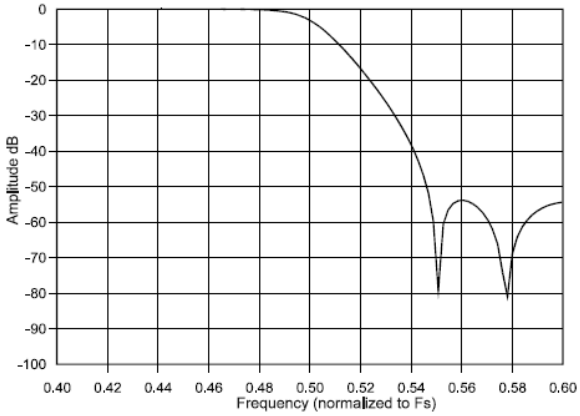
(2) To prevent audio transients at power-down the DC-blocking capacitors must fully discharge before turning off the power. In order to do this MCLKIN should be stopped for a period of about 250 ms for a 3.3 µF cap connected to VQ (420 ms for a 10 µF cap connected to VQ) before removing power. During this time voltage on VQ and the audio outputs discharge gradually to GND.

5.10.2 Analog Output and Filtering

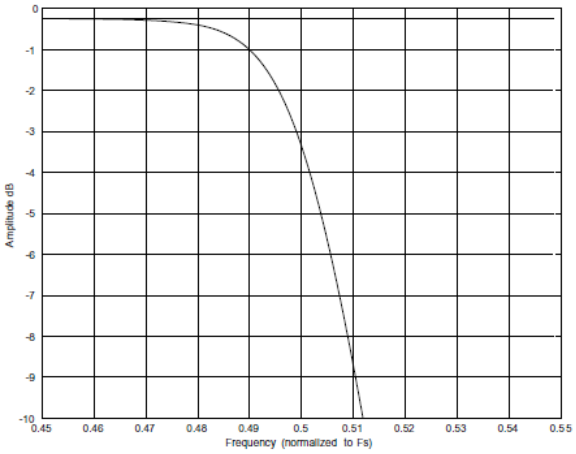
The analog filter present in the MS8412 is a switched-capacitor filter followed by a continuous time low pass filter. Its response, combined with that of the digital interpolator, is given in Figures.



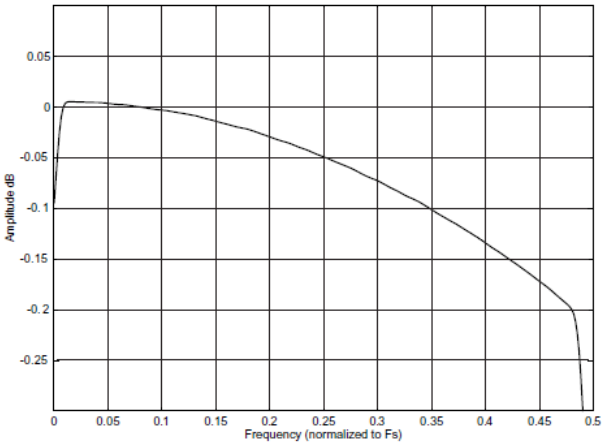
Single-Speed Stopband Rejection



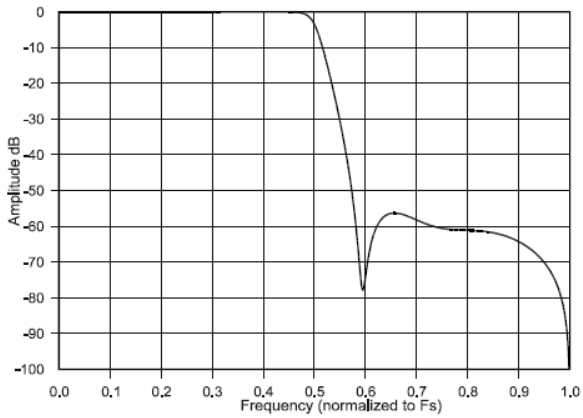
Single-Speed Transition Band



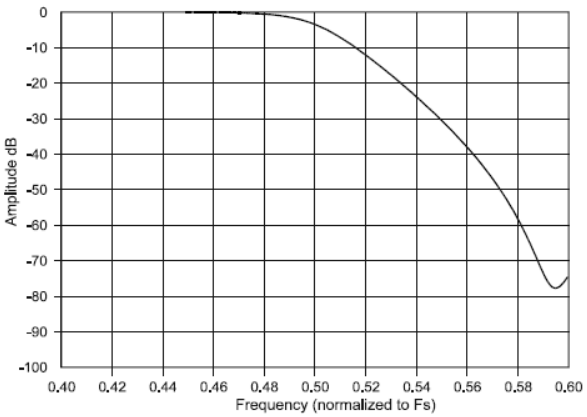
Single-Speed Transition Band



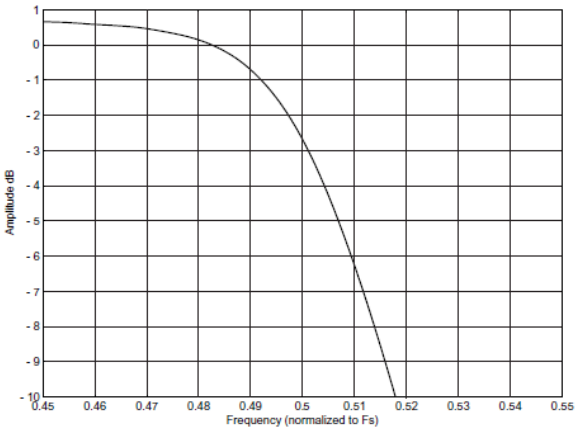
Single-Speed Passband Ripple



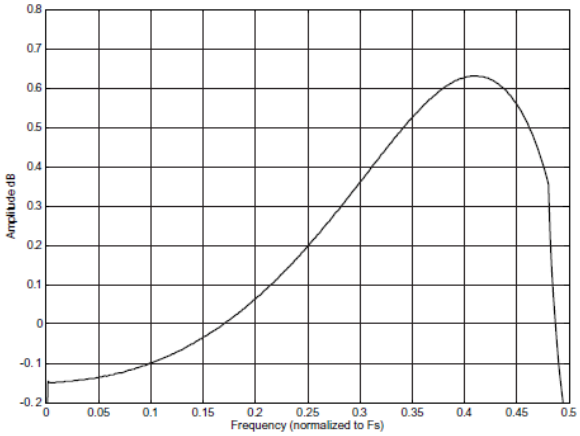
Double-Speed Stopband Rejection



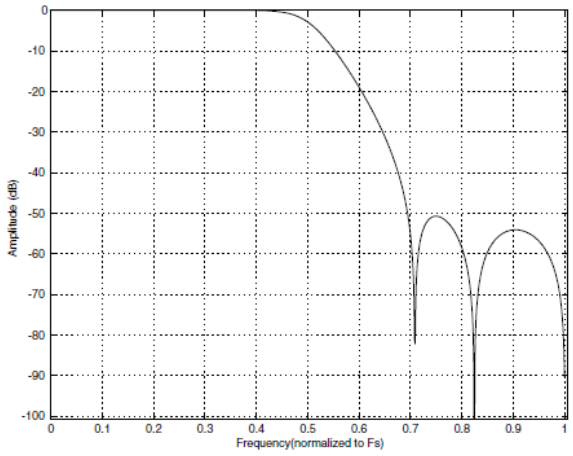
Double-Speed Transition Band



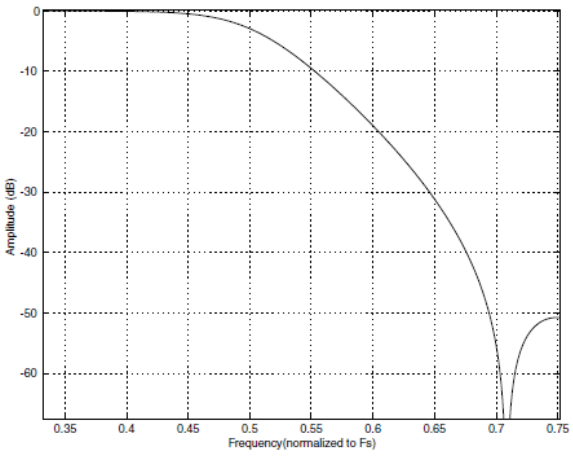
Double-Speed Transition Band



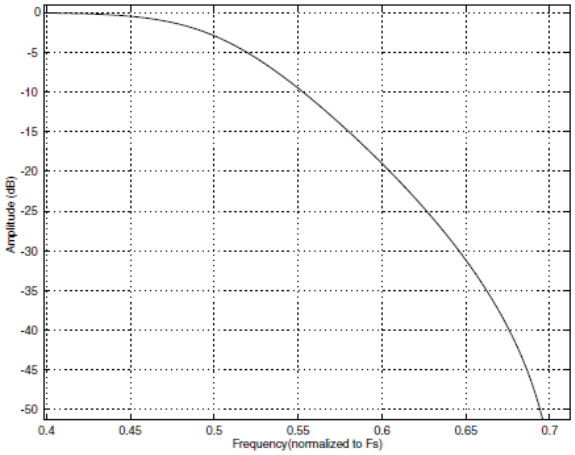
Double-Speed Passband Ripple



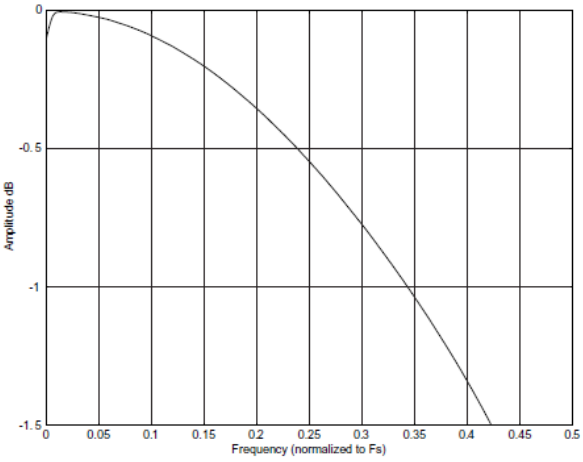
Quad-Speed Stopband Rejection



Quad-Speed Transition Band



Quad-Speed Transition Band



Quad-Speed Passband Ripple

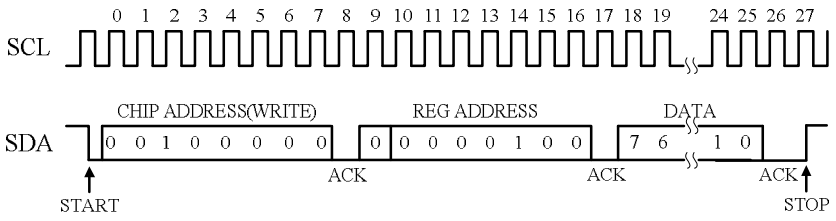
6、CONTROL PORT DESCRIPTION

MS8412 supports I²C interface.

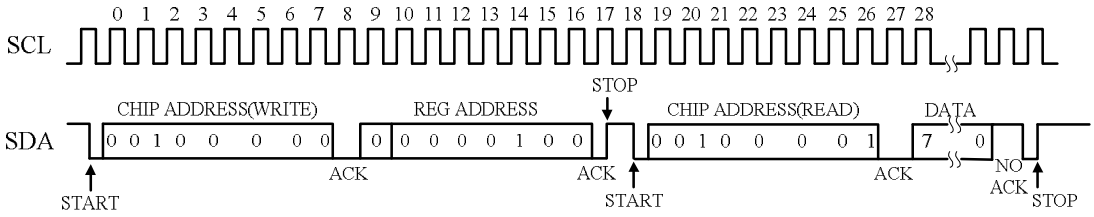
6.1 I²C

SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. The states of the pins are sensed while the MS8412 is being reset.

The signal timings for a read and write cycle are shown in following Figures. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the MS8412 after a Start condition consists of a 7-bit chip address field and a R/W bit (high for a read, low for a write). The 7-bit address field are fixed at 0010000. To communicate with a MS8412, the chip address field, which is the first byte sent to the MS8412. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the address of register(04h). If the operation is a read, the contents of the register 04h will be output. Each byte is separated by an acknowledge bit (ACK). The ACK bit is output from the MS8412 after each input byte is read, and is input to the MS8412 from the microcontroller after each transmitted byte.



Control Port Timing, I²C Slave Mode Write



Control Port Timing, I²C Slave Mode Read

6.1 Multiplexer control(04h)

7	6	5	4	3	2	1	0
1	0	RXSEL2	RXSEL1	RXSEL0	0	0	0

RXSEL[2:0] - Selects RXP0 to RXP3 for input to the receiver

Default =’000’

000 – RXP0

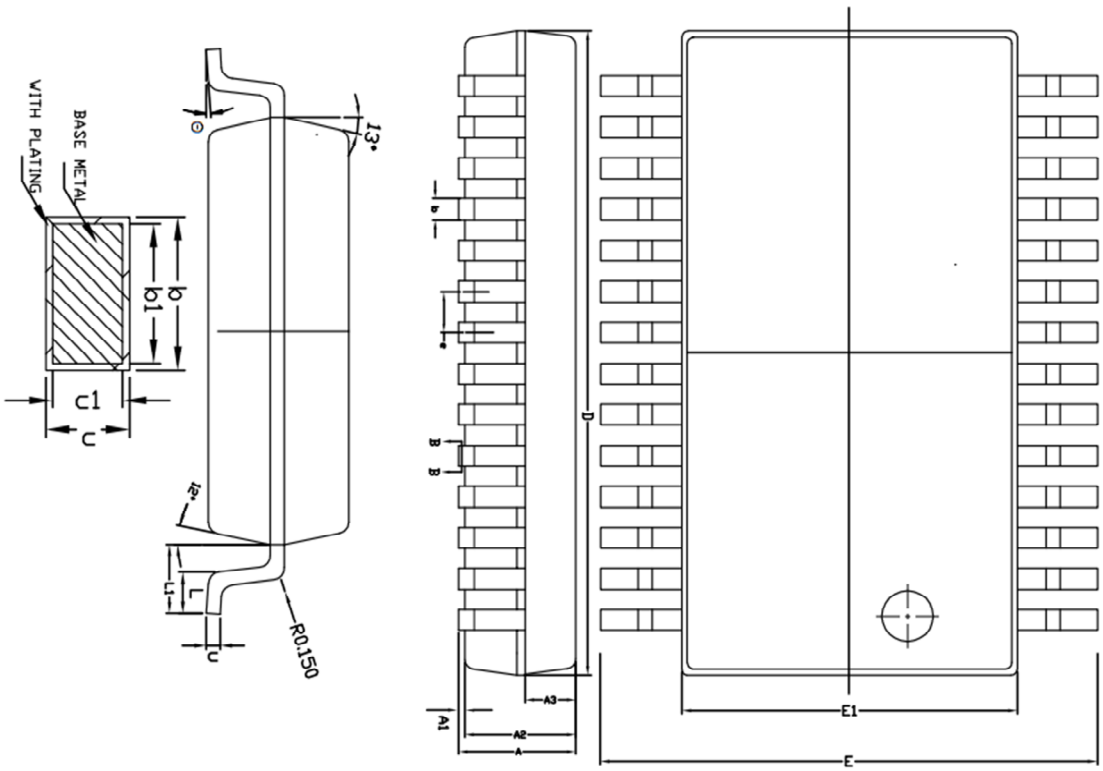
001 – RXP1,

010 – RXP2

011 – RXP3

PACKAGE OUTLINE DIMENSIONS

SSOP28 UNIT: mm



DIM / SYMBOL	MIN.	NOM.	MAX.
A	–	–	2.00
A1	0.05	–	0.25
A2	1.65	1.75	1.85
A3	0.75	0.80	0.85
b	0.29	–	0.37
b1	0.28	0.30	0.33
c	0.15	–	0.20
c1	0.14	0.15	0.16
D	10.00	10.20	10.40
E	7.60	7.80	8.00
E1	5.10	5.30	5.50
e	0.65BSC		
L	0.55	0.75	0.95
L1	1.25BSC		
θ	0°	–	8°

Marking drawing criterion and packing instruction

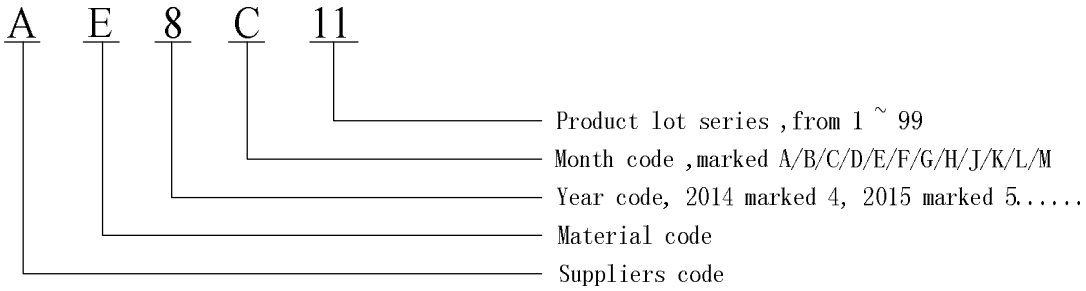
TOP VIEW

1. Marking drawing criterion

MS8412: product name

Lot No:

Example: AE8C11



2. Marking drawing pattern

Laser printing, contents in the middle, font type Arial

3.Packing instruction

Type	piece/roll	roll/box	piece/box	box/carton	piece/carton
MS8412	2000	1	2000	8	16000