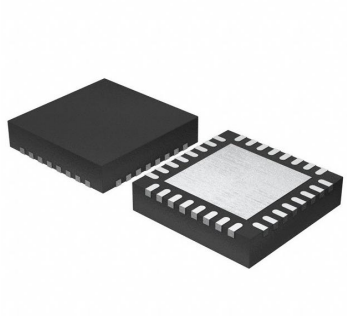
The Contact-less Card Reader IC

PRODUCT DESCRIPTION

The MS512 is a highly integrated reader/writer for contact-less communication at 13.56 MHz. It utilizes an outstanding modulation and demodulation concept completely integrated for different kinds of contactless communication methods and protocols at 13.56 MHz.

FEATURES

- Highly integrated analog circuit to demodulate and decode
- Minimum external components used to drive an antenna
- Supports ISO/IEC 14443 A, ISO/IEC 14443 B and FeliCa Read/Write mode
- Supports ISO/IEC 14443 A card or FeliCa Card Operation mode
- Supports NFCIP-1 mode
- Up to 50mm operating distance in Read/Write mode depending on the antenna design
- Supports the following host interfaces: SPI, I^2C, RS232 Serial UART, 8-bit parallel interface
- FIFO buffer handles 64 byte send and receive
- Flexible interrupt modes
- Hard reset with low power function
- Power-down by software mode
- Programmable timer
- Internal oscillator for connection to 27.12 MHz quartz crystal
- Operates from 2.7V to 3.3V single power supply
- CRC coprocessor
- Programmable I/O pins
- Internal self-test



QFN32

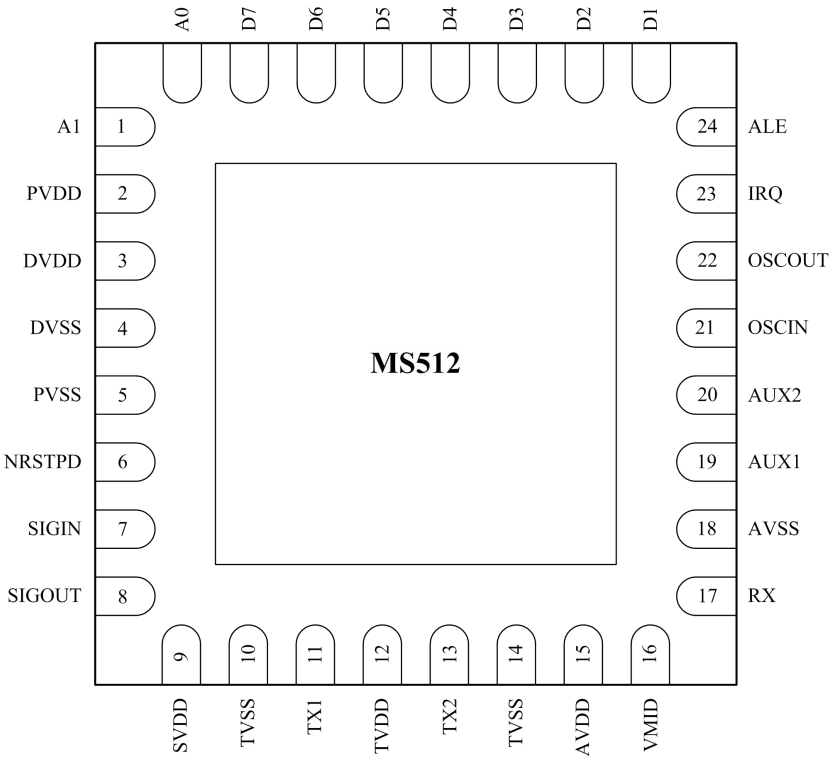
APPLICATIONS

- Portable hand-held devices
- Public transport terminal
- Contact-less public telephone
- Intelligent electric meter reading

PACKAGE SPECIFICATION

Part Number	Package	Marking
MS512	QFN32	MS512
MS512	QFN40	MS512F

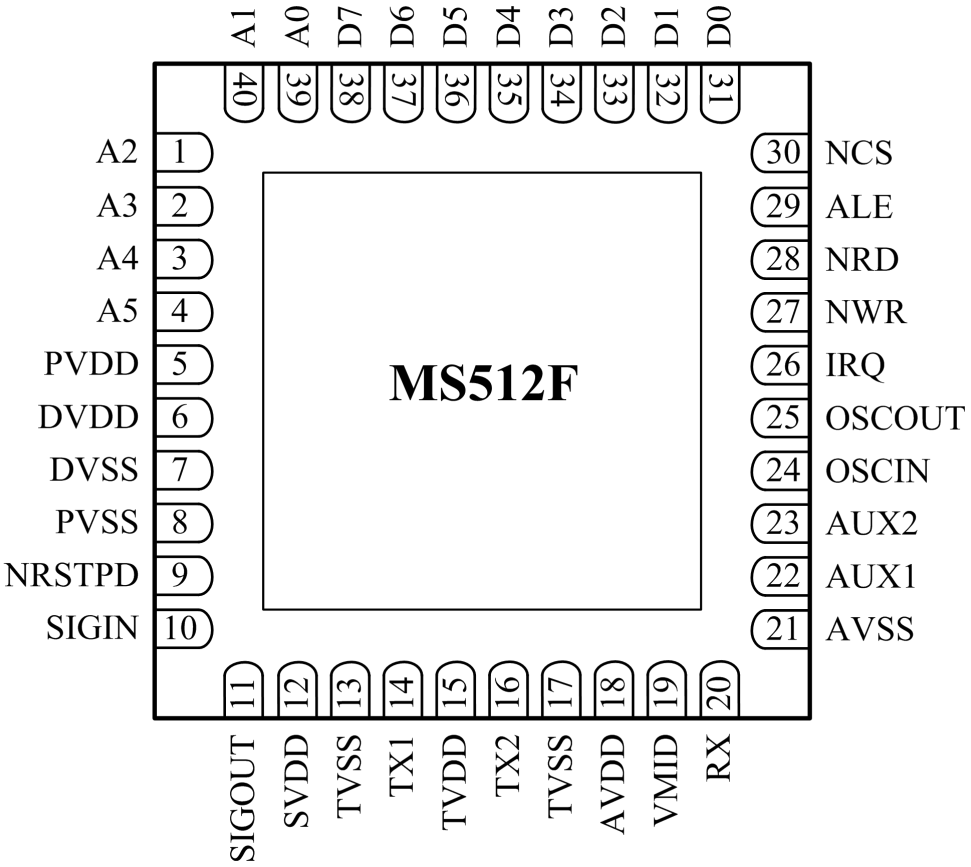
PIN CONFIGURATION - QFN32



Pin	Symbol	Type	Description
1	A1	I	address
2	PVDD	P	pin power supply
3	DVDD	P	digital power supply
4	DVSS	G	digital ground
5	PVSS	G	pin power supply ground
6	NRSTPD	I	reset and power-down input: reset:enabled by a positive edge power-down:enabled when LOW;internal current sinks are switched off, the oscillator is inhibited and the input pins are disconnected from the outside world
7	SIGIN	I	S2C signal input
8	SIGOUT	O	S2C signal output
9	SVDD	P	SIGIN and SIGOUT pins power supply
10	TVSS	G	transmitter output stage 1 ground
11	TX1	O	transmitter 1 modulated 13.56 MHz energy carrier output
12	TVDD	P	transmitter power supply: supplies the output stage of transmitters 1 and 2
13	TX2	O	transmitter 2 modulated 13.56 MHz energy carrier output
14	TVSS	G	transmitter output stage 2 ground
15	AVDD	P	analog power supply
16	VMID	P	internal reference voltage
17	RX	I	RF signal input
18	AVSS	G	analog ground
19	AUX1	O	auxiliary outputs for test purposes
20	AUX2	O	auxiliary outputs for test purposes
21	OSCIN	I	crystal oscillator inverting amplifier input;also the input for an externally generated clock(f_{OSC}=27.12MHz)
22	OSCOUT	O	crystal oscillator inverting amplifier output

23	IRQ	O	interrupt request output : indicates an interrupt event
24	ALE	I	address latch enable
25-31	D1-D7	I/O	8-bit bi-directional data bus
32	A0	I	address

PIN CONFIGURATION - QFN40



Pin	Symbol	Type	Description
1-4	A2-A5	I	address
5	PVDD	P	pin power supply
6	DVDD	P	digital power supply
7	DVSS	G	digital ground
8	PVSS	G	pin power supply ground
9	NRSTPD	I	reset and power-down input: reset:enabled by a positive edge power-down:enabled when LOW;internal current sinks are switched off, the oscillator is inhibited and the input pins are disconnected from the outside world
10	SIGIN	I	S2C signal input
11	SIGOUT	O	S2C signal output
12	SVDD	P	SIGIN and SIGOUT pins power supply
13	TVSS	G	transmitter output stage 1 ground
14	TX1	O	transmitter 1 modulated 13.56 MHz energy carrier output
15	TVDD	P	transmitter power supply: supplies the output stage of transmitters 1 and 2
16	TX2	O	transmitter 2 modulated 13.56 MHz energy carrier output
17	TVSS	G	transmitter output stage 2 ground
18	AVDD	P	analog power supply
19	VMID	P	internal reference voltage
20	RX	I	RF signal input
21	AVSS	G	analog ground

22	AUX1	O	auxiliary outputs for test purposes
23	AUX2	O	auxiliary outputs for test purposes
24	OSCIN	I	crystal oscillator inverting amplifier input;also the input for an externally generated clock(f_{OSC}=27.12MHz)
25	OSCOUT	O	crystal oscillator inverting amplifier output
26	IRQ	O	interrupt request output : indicates an interrupt event
27	NWR	I	strobe to write data into the register
28	NRD	I	strobe to read data from the register
29	ALE	I	address latch enable
30	NCS	I	selects and activates the host controller interface
31-38	D1-D7	I/O	8-bit bi-directional data bus
39-40	A0-A1	I	address

BLOCK DIAGRAM

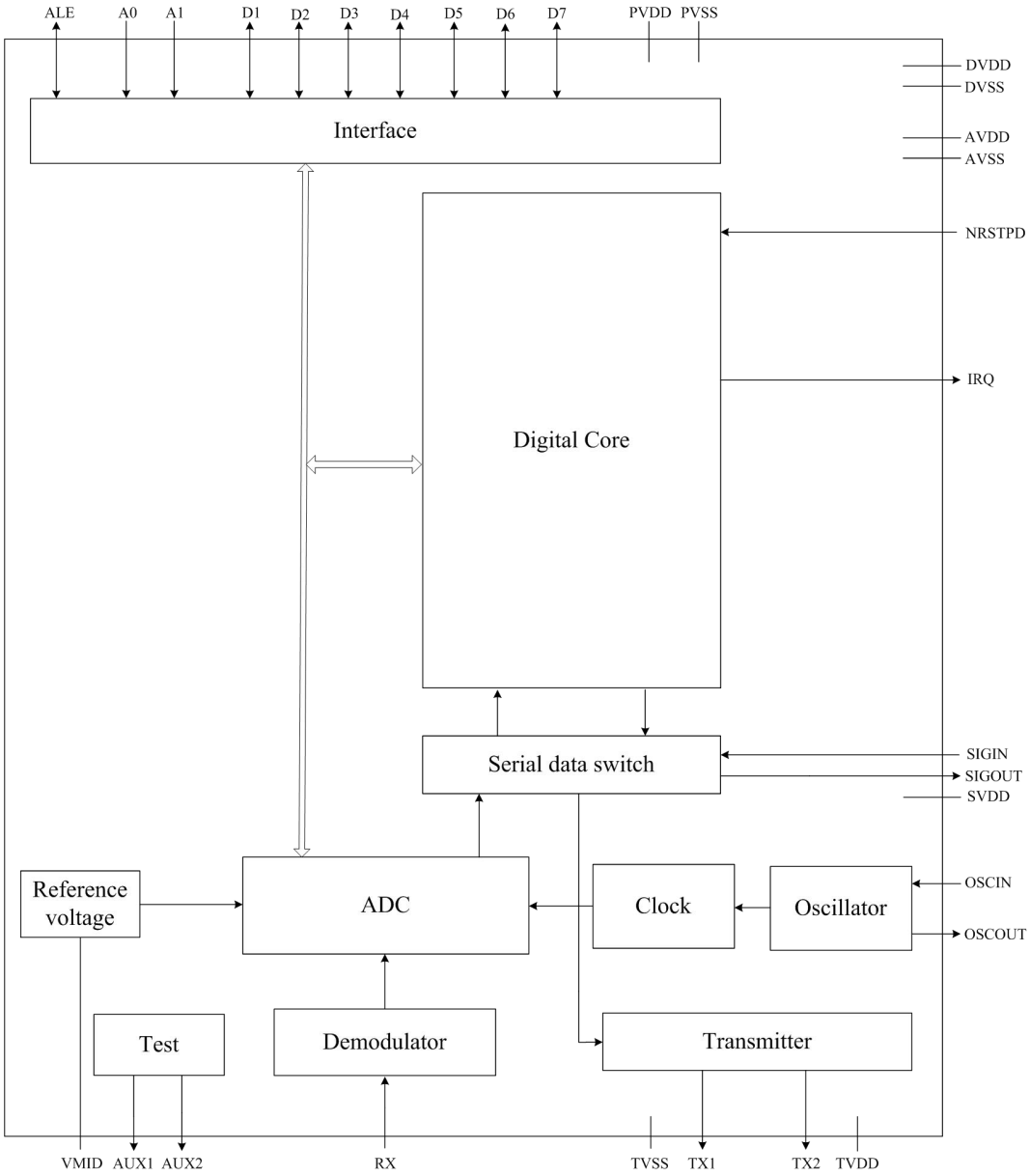


Figure 1. block diagram

ABSOLUTE MAXIMUM RATINGS

Stresses below those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions below those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1 Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		-0.5	+4.0	V
V_{DDD}	digital supply voltage		-0.5	+4.0	V
$V_{DD(PVDD)}$	PVDD supply voltage		-0.5	+4.0	V
$V_{DD(TVDD}$	TVDD supply voltage		-0.5	+4.0	V
$V_{DD(SVDD}$	SVDD supply voltage		-0.5	+4.0	V
V_I	Input voltage	all input pins except pins TIN and RX	$V_{SS(PVSS)}$-0.5	$V_{DD(PVDD)}$-0.5	V
		pin TIN	$V_{SS(PVSS)}$-0.5	$V_{DD(SVDD)}$-0.5	V
P_{tot}	total dissipation	per package;V_{DDD} in shortcut mode	-	200	mW
T_j	junction temperature		-	100	℃
V_{ESD}	electrostatic discharge voltage	HBM；150Ω,100pF；JESD22-A144-B	-	5000	V
		MM；0.75μH,200pF；JESD22-A144-A	-	300	V

Electrical Characteristics

Table 2.Operating Condition

Symbol	Parameter	Conditions	Min	Typ	Max	Uni
V_{DDA}	analog supply voltage	$V_{DD(PVDD)} \le V_{DDA}=V_{DDD}=V_{DD(TVDD)}$; [1][2] $V_{SSA}=V_{SSD}=V_{SS(PVSS)}=V_{SS(TVSS)}=0V$	2.5	3.3	3.6	V
V_{DDD}	digital supply voltage	$V_{DD(PVDD)} \le V_{DDA}=V_{DDD}=V_{DD(TVDD)}$; [1][2] $V_{SSA}=V_{SSD}=V_{SS(PVSS)}=V_{SS(TVSS)}=0V$	2.5	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage	$V_{DD(PVDD)} \le V_{DDA}=V_{DDD}=V_{DD(TVDD)}$; [1][2] $V_{SSA}=V_{SSD}=V_{SS(PVSS)}=V_{SS(TVSS)}=0V$	2.5	3.3	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage	$V_{DD(PVDD)} \le V_{DDA}=V_{DDD}=V_{DD(TVDD)}$; [3] $V_{SSA}=V_{SSD}=V_{SS(PVSS)}=V_{SS(TVSS)}=0V$	1.6	1.8	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA}=V_{SSD}=V_{SS(PVSS)}=V_{SS(TVSS)}=0V$	1.6	-	3.6	V
T_{amb}	ambient temperature		-40	-	+100	℃

[1] Supplyvoltagesbelow3Vreducetheperformancein,for example,the achievable operating distance.

[2] V_{DDA},V_{DDD} and $V_{DD(TVDD)}$ must always be the same voltage.

[3] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DDD}.

Table 3. Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input characteristics						
Pins A0, A1 and NRSTPD						
I_{LI}	Input leakage current		-1	-	+1	A
V_{IH}	HIGH-level input voltage		$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(PVDD)}$	V
Pin SIGIN						
I_{LI}	input leakage current		-1	-	+1	A
V_{IH}	HIGH-level input voltage		$0.7V_{DD(SVDD)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(SVDD)}$	V
Pin ALE						
I_{LI}	Input leakage current		-1	-	+1	A
V_{IH}	HIGH-level input voltage		$0.7V_{DD(PVDD)}$	-	-	V
V_{I_L}	LOW-level input voltage		-	-	$0.3V_{DD(PVDD)}$	V
Pin RX						
V_i	Input voltage		-1	-	$V_{DDA}+1$	V
C_i	Input capacitance	VDDA=3 V;receiver active; VRX(p-p)=1V;1.5V(DC) offset	-	10	-	pF

R_i	Input resistance	VDDA=3 V;receiver active; VRX(p-p)=1V;1.5V(DC) offset	-	350	-	
Input voltage range						
$V_{i(p-p)(min)}$	minimum peak-to-peak input voltage	Manchester encoded; VDDA=3V	-	100	-	mV
$V_{i(p-p)(max)}$	maximum peak-to-peak input voltage	Manchester encoded; VDDA=3V	-	4	-	V
Input sensitivity						
Vmod	modulation voltage	Minimum Manchester encoded;VDDA=3V RxGain=11b (48dB)	-	5	-	mV
Pin OSCIN						
I_{LI}	Input leakage current		-1	-	+1	A
V_{IH}	HIGH-level input voltage		$0.7V_{DDA}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DDA}$	V
C_i	Input capacitance	VDDA= 2.8V;DC=0.65V; AC=1V (p-p)	-	2	-	pF
Input/output characteristics						
Pins D1,D2,D3,D4,D5,D6 and D7						
I_{LI}	Input leakage current		-1	-	+1	A
V_{IH}	HIGH-level input voltage		$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(PVDD)}$	V
V_{OH}	HIGH-level output voltage	VDD(PVDD)=3V; I_O=4mA	$V_{DD(PVDD)}$-0.4	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	VDD(PVDD)=3V; I_O=4mA	$V_{SS(PVSS)}$	-	$V_{SS(PVDD)}$ + 0.4	V
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$= 3 V	-	-	4	mA
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$= 3 V	-	-	4	mA
Output characteristics						
Pin SIGOUT						
V_{OH}	HIGH-level output voltage	$V_{DD(SVDD)}$= 3V;I_O= 4mA	$V_{DD(SVDD)}$-0.4	-	VDD(SVDD)	V
V_{OL}	LOW-level output voltage	$V_{DD(SVDD)}$= 3V;I_O= 4mA	$V_{SS(PVSS)}$	-	VSS(PVSS) +0.4	V
I_{OL}	LOW-level output current	$V_{DD(SVDD)}$= 3 V	-	-	4	mA
I_{OH}	HIGH-level output current	$V_{DD(SVDD)}$= 3 V	-	-	4	mA
Pin IRQ						

V_{OH}	HIGH-level output voltage	$V_{DD(PVDD)}$= 3V; I_O= 4mA	$V_{DD(PVDD)}$-0.4	-	VDD(PVDD)	V
V_{OL}	LOW-level output voltage	$V_{DD(PVDD)}$= 3V; I_O= 4mA	$V_{SS(PVSS)}$	-	VSS(PVSS) +0.4	V
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$= 3 V	-	-	4	mA
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$= 3 V	-	-	4	mA
Pins AUX1 and AUX2						
V_{OH}	HIGH-level output voltage	V_{DDD}= 3V;I_O= 4mA	V_{DDD}-0.4	-	VDDD	V
V_{OL}	LOW-level output voltage	V_{DDD}= 3V;I_O= 4mA	$V_{SS(PVSS)}$	-	VSS(PVSS) +0.4	V
I_{OL}	LOW-level output current	V_{DDD}= 3 V	-	-	4	mA
I_{OH}	HIGH-level output current	V_{DDD}= 3 V	-	-	4	mA
Pins TX1 and TX2						
V_{OH}	high-level output voltage	$V_{DD(TVDD)}$=3V; $I_{DD(TVDD)}$=32mA; CWGsP=3Fh	$V_{DD(TVDD)}$-0.15	-	-	V
		$V_{DD(TVDD)}$=3V;IDD(TVDD)=80mA; CWGsP=3Fh	$V_{DD(TVDD)}$-0.4	-	-	V
		$V_{DD(TVDD)}$=2.5V; $I_{DD(TVDD)}$=32mA; CWGsP=3Fh	$V_{DD(TVDD)}$-0.24	-	-	V
		$V_{DD(TVDD)}$=2.5V; $I_{DD(TVDD)}$=80mA; CWGsP=3Fh	$V_{DD(TVDD)}$-0.64	-	-	V
V_{OL}	low-level output voltage	$V_{DD(TVDD)}$=3V; $I_{DD(TVDD)}$=32mA; CWGsP=0Fh	-	-	0.15	V
		$V_{DD(TVDD)}$=3V; $I_{DD(TVDD)}$=80mA; CWGsP=0Fh	-	-	0.4	V
		$V_{DD(TVDD)}$=2.5V; $I_{DD(TVDD)}$=32mA; CWGsP=0Fh	-	-	0.24	V
		$V_{DD(TVDD)}$=2.5V; $I_{DD(TVDD)}$=80mA; CWGsP=0Fh	-	-	0.64	V
Current consumption						
I_{pd}	power-down current	V_{DDA}=V_{DDD}=$V_{DD(TVDD)}$=$V_{DD(PVDD)}$ =3V				
		hard-power-down; Pin NRSTPD set LOW	-	-	5	A
		Soft-power-down; RF level detector on	-	-	10	A
I_{DDD}	digital supply current	Pin DVDD; V_{DDD}= 3 V	-	6.5	9	mA
I_{DDA}	analog supply current	pin AVDD; V_{DDA}=3V; CommandReg register's bit RcvOff =0	-	7	10	mA
		pin AVDD; receiver switched-off; V_{DDA}=3V; CommandReg register's bit RcvOff =1	-	3	5	mA

$I_{DD(PVDD)}$	PVDD supply current	pin PVDD	-	-	40	mA
$I_{DD(TVDD)}$	TVDD supply current	Pin TVDD; continuous wave	-	60	100	mA
$I_{DD(SVDD)}$	SVDD supply current	pin SVDD	-	-	4	mA
Clock frequency						
f_{clk}	clock frequency		-	27.12	-	MHz
clk	clock duty cycle		40	50	60	%
t_{jit}	jitter time	RMS	-	-	10	ps
Crystal oscillator						
V_{OH}	HIGH-level output voltage	pin OSCOUT	-	1.1	-	V
V_{OL}	LOW-level output voltage	pin OSCOUT	-	0.2	-	V
C_i	Input capacitance	pin OSCOUT	-	2	-	pF
		pin OSCIN	-	2	-	pF
Typical input requirements						
f_{xtal}	crystal frequency		-	27.12	-	MHz
ESR	equivalent series resistance		-	-	100	Ω
C_L	load capacitance		-	10	-	pF
P_{xtal}	crystal power dissipation		-	50	100	uW

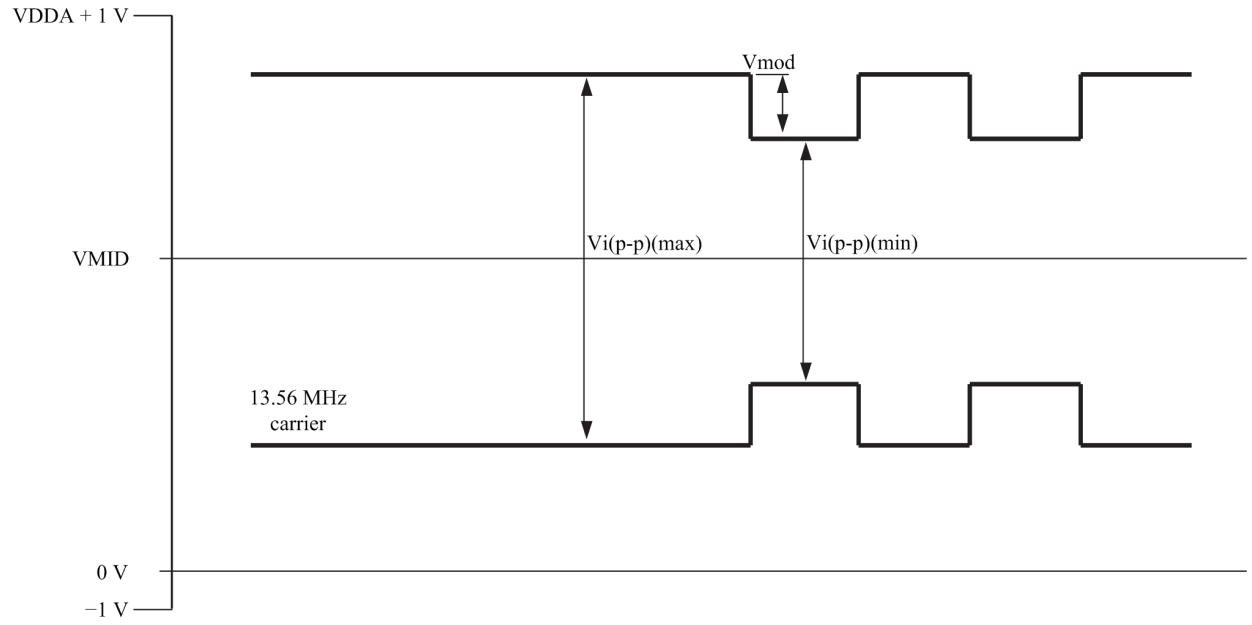


Figure 2. Pin RX input voltage range

Function Description

The MS512 transmission module supports ISO/IEC 14443 A and ISO/IEC 14443 B Read/Write mode at various transfer speeds and modulation protocols.

MS512 supports the operating modes:

1.Reader/Writer mode supporting ISO/IEC 14443A, ISO/IEC 14443B and FeliCa

2.Card Operation mode supporting ISO/IEC 14443A and FeliCa

3.NFCIP-1 mode

1.1 ISO/IEC 14443 A functionality

The physical level communication is shown in Figure 3.

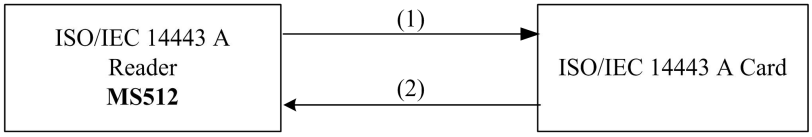


Figure 3. ISO/IEC 14443 A Read/Write mode communication

The physical parameters are described in Table 4.

Table 4. Communication overview for ISO/IEC 14443 A reader/writer

Communication direction	Signal type	Transfer speed			
		106 kBd	212 kBd	424 kBd	848 kBd
Reader to card (MS512 sends data to a card	reader side modulation	100 % ASK	100 % ASK	100 % ASK	100 % ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding
	bit length	128 (13.56 us)	64 (13.56 us)	32 (13.56 us)	16 (13.56 us)
Card to reader (card sends data to the MS512)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56MHz/16	13.56MHz/16	13.56MHz/16	13.56MHz/16
	bit encoding	Manchester encoding	BPSK	BPSK	BPSK

MS512's contact-less UART and dedicated external host must manage the ISO/IEC 14443 A protocol. The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally based on the transfer speed.

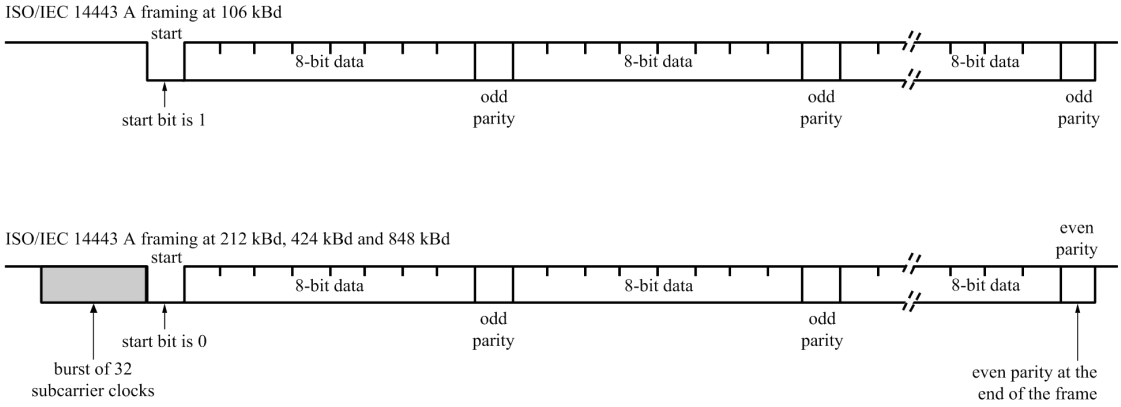


Figure 4. Data coding and framing according to ISO/IEC 14443 A

1.2 ISO/IEC 14443 B functionality

The MS512 reader IC fully supports the ISO 14443 international standard which includes the communication schemes ISO 14443 A and ISO 14443 B.

1.3 FeliCa functionality

The FeliCa mode is the general reader/writer to card communication scheme according to the FeliCa specification.

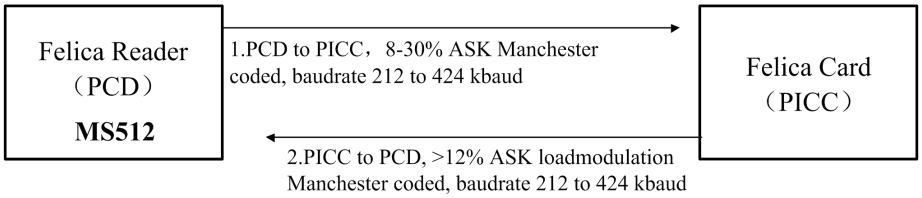


Figure 5. FeliCa reader/writer communication diagram

Table 5. Communication overview for FeliCa reader/writer

Communication direction		FeliCa	FeliCa Higher transfer speeds
	Transfer speed	212 kbit/s	424 kbit/s
MS512 to card	modulation on reader side	8-30% ASK	8-30% ASK
	bit coding	Manchester Coding	Manchester Coding
	bit length	(64/13.56)us	(32/13.56)us
card to MS512	loadmodulation on card side	> 12% ASK	> 12% ASK
	bit coding	Manchester coding	Manchester coding

1.3.1 FeliCa framing and coding

Table 6. FeliCa framing and coding

Preamble						Sync		Len	n-Data				CRC	
00h	00h	00h	00h	00h	00h	B2h	4Dh	-	-	-	-	-	-	-

To enable the FeliCa communication a 6 byte preamble (00h, 00h, 00h, 00h, 00h, 00h) and 2 bytes Sync bytes (B2h, 4Dh) are sent to synchronize the receiver. The following Len byte indicates the length of the sent data bytes plus the LEN byte itself. The CRC calculation is done according to the FeliCa definitions with the MSB first.

To transmit data on the RF interface, the host controller has to send the Len and data bytes to the MS512's FIFO. The preamble and the sync bytes are generated by the MS512 automatically and must not be written to the FIFO by the host controller. The MS512 performs internally the CRC calculation and adds the result to the data frame.

Example for FeliCa CRC Calculation:

Table 7. Start value for the CRC Polynomial

Preamble						Sync		Len	Data Bytes		CRC	
00h	00h	00h	00h	00h	00h	B2h	4Dh	03h	ABh	CDh	90h	35h

1.4 NFCIP-1 mode

The NFCIP-1 communication differentiates between an active and a Passive Communication mode.

1.Active Communication mode means both the initiator and the target are using their own RF field to transmit data.

2.Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active in terms of generating the RF field.

3.Initiator: generates RF field at 13.56 MHz and starts the NFCIP-1 communication.

4.Target: responds to initiator command either in a load modulation scheme in Passive Communication mode or using a self generated and self modulated RF field for Active Communication mode.

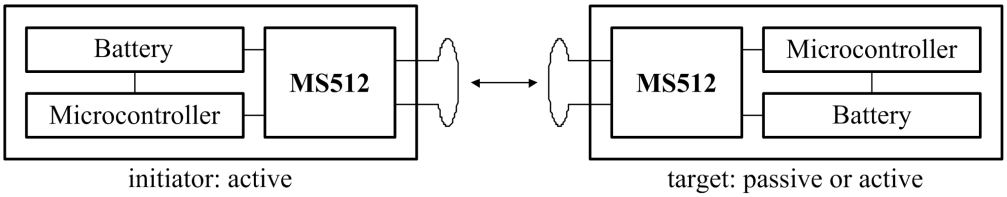


Figure 6. NFCIP-1 mode

1.4.1 Active communication mode

Active communication mode means both the initiator and the target are using their own RF field to transmit data.

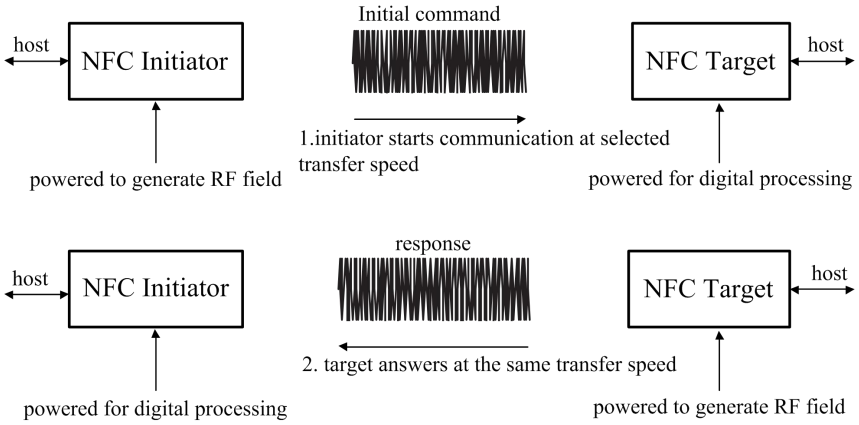


Figure 7. Active communication mode

Table 8. Communication overview for Active communication mode

Communication direction	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s	1.69 Mbit/s, 3.39 Mbit/s
Initiator to Target	According to ISO/IEC 14443A 100% ASK, Modified Miller Coded	According to FeliCa, 8-30% ASK Manchester Coded		digital capability to handle this communication	
Target to Initiator					

1.4.2 Passive communication mode

Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active meaning generating the RF field.

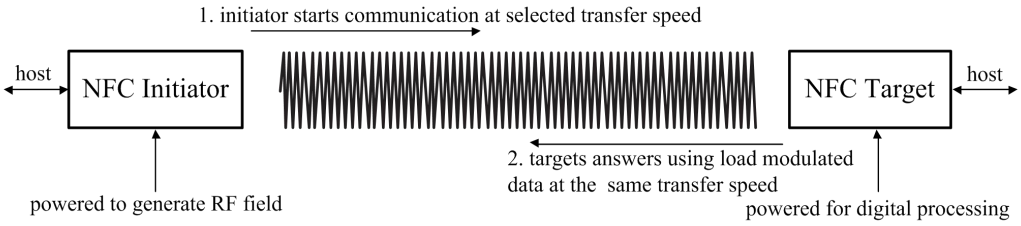


Figure 8. Passive communication mode

Table 9. Communication overview for Passive communication mode

Communication direction	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s	1.69 Mbit/s, 3.39 Mbit/s
Initiator to Target	According to ISO/IEC 14443A 100% ASK, Modified Miller Coded	According to FeliCa, 8-30% ASK Manchester Coded		digital capability to handle this communication	
Target to Initiator	According to ISO/IEC 14443A subcarrier load modulation, Manchester Coded	According to FeliCa, > 12% ASK Manchester Coded			

1.4.3 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Active and Passive Communication mode is defined in the NFCIP-1 standard.

Table 10. Framing and coding overview

Transfer speed	Framing and Coding
106 kbit/s	According to the ISO/IEC 14443A scheme
212 kbit/s	According to the FeliCa scheme
424 kbit/s	According to the FeliCa scheme

1.4.4 ISO/IEC 14443A Card operation mode

Table 11. ISO/IEC 14443A Card operation mode

Communication direction		ISO/IEC 14443A	Higher transfer speeds	
	transfer speed	106 kbit/s	212 kbit/s	424 kbit/s
reader/writer to MS512	Modulation on reader side	100 % ASK	100 % ASK	100 % ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller
	bit length	(128/13.56) us	(64/13.56) us	(32/13.56) us
MS512 to reader/writer	Modulation on MS512 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester coding	BPSK	BPSK

1.4.5 FeliCa Card operation mode

Table 12. FeliCa Card operation mode

Communication direction		FeliCa	Higher transfer speeds
	transfer speed	212 kbit/s	424 kbit/s
reader/writer to MS512	Modulation on reader side	8-30 % ASK	8-30 % ASK
	bit coding	Manchester coding	Manchester coding
	bit length	(64/13.56) us	(32/13.56) us
MS512 to reader/writer	Load modulation on MS512 side	>12% ASK load modulation	>12% ASK load modulation
	bit coding	Manchester coding	Manchester coding

1.5 Digital interfaces

1.5.1 Automatic microcontroller interface detection

The MS512 supports direct interfacing to hosts using SPI, I²C-bus or serial UART interfaces. The MS512 resets its interface and checks the current host interface type automatically after performing a power-on or hard reset.

The MS512 identifies the host interface by sensing the logic levels on the control pins after the reset phase. This is done using a combination of fixed pin connections.

Table 13. Connection protocol for detecting different interface types

Pin	Parallel Interface Type				Serial Interface Types		
	Separated Read/Write Strobe		Common Read/Write Strobe				
	Dedicated Address Bus	Multiplexed Address Bus	Dedicated Address Bus	Multiplexed Address Bus	UART	SPI	I²C
ALE	1	ALE	1	AS	RX	NSS	SDA
A5[1]	A5	0	A5	0	0	0	0
A4[1]	A4	0	A4	0	0	0	0
A3[1]	A3	0	A3	0	0	0	0
A2[1]	A2	1	A2	1	0	0	0
A1	A1	1	A1	1	0	0	1
A0	A0	1	A0	0	0	1	EA
NRD[1]	NRD	NRD	NDS	NDS	1	1	1
NWR[1]	NWR	NWR	RD/NWR	RD/NWR	1	1	1
NCS[1]	NCS	NCS	NCS	NCS	NCS	NCS	NCS
D7	D7	D7	D7	D7	TX	MISO	SCL
D6	D6	D6	D6	D6	MX	MOSI	ADR_0
D5	D5	AD5	D5	AD5	DTRQ	SCK	ADR_1
D4	D4	AD4	D4	AD4	-	-	ADR_2
D3	D3	AD3	D3	AD3	-	-	ADR_3
D2	D2	AD2	D2	AD2	-	-	ADR_4
D1	D1	AD1	D1	AD1	-	-	ADR_5
D0	D0	AD0	D0	AD0	-	-	ADR_6

[1] only available in QFN40.

1.5.2 Serial Peripheral Interface

Serial Peripheral Interface (SPI) is supported and enables high-speed communication with the host. The interface can manage data speeds up to 10 Mbit/s. When communicating with a host, the MS512 acts as a slave. As such, it receives data from the external host for register settings, sends and receives data relevant for RF interface communication.

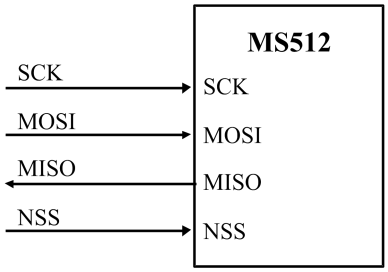


Figure 9. SPI connection to host

The MS512 acts as a slave during SPI communication and is timed using the SPI clock signal (SCK) generated by the

master. Data communication from the master to the slave uses the MOSI line. The MISO line is used to send data from the MS512 to the master.

Data bytes on both MOSI and MISO lines are sent with the MSB first. Data on both MOSI and MISO lines must be stable on the rising edge of the clock and can be changed on the falling edge. Data is sent by the MS512 on the falling clock edge and is stable during the rising clock edge.

1.5.3 UART interface

1.5.3.1 Connection to a host

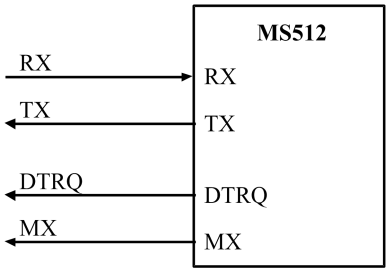


Figure 10. UART connection to microcontrollers

1.5.3.2 Selectable UART transfer speeds

The internal UART interface is compatible with the RS232 serial interface.

The default transfer speed is 9.6 kBd. To change the transfer speed, the host controller must write a value for the new transfer speed to the register.

1.5.4 I²C Bus Interface

An I²C-bus interface is supported and enables implementation of a low-cost, low pin count serial bus interface to the host. The interface can only act in slave mode. Therefore the MS512 does not perform clock generation or access arbitration.

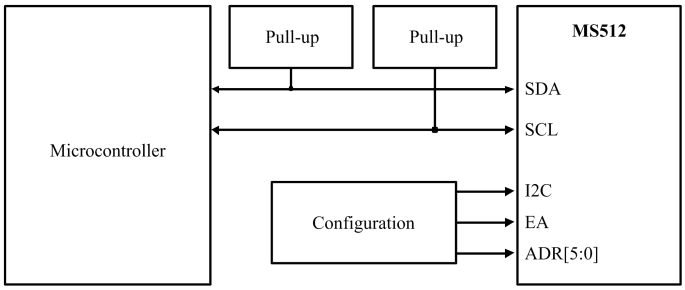


Figure 11. I²C-bus interface

SDA is a bidirectional line connected to a positive supply voltage using a current source or a pull-up resistor. Both SDA and SCL lines are set HIGH when data is not transmitted. The MS512 has a 3-state output stage to perform the wired-AND function. Data on the I²C-bus can be transferred at data rates of up to 100 kBd in Standard mode, up to 400 kBd in Fast mode or up to 3.4 Mbit/s in High-speed mode.

If the I²C-bus interface is selected, spike suppression is activated on lines SCL and SDA as defined in the I²C-bus interface specification.

1.6 8-bit parallel interface

1.6.1 Separated Read/Write strobe

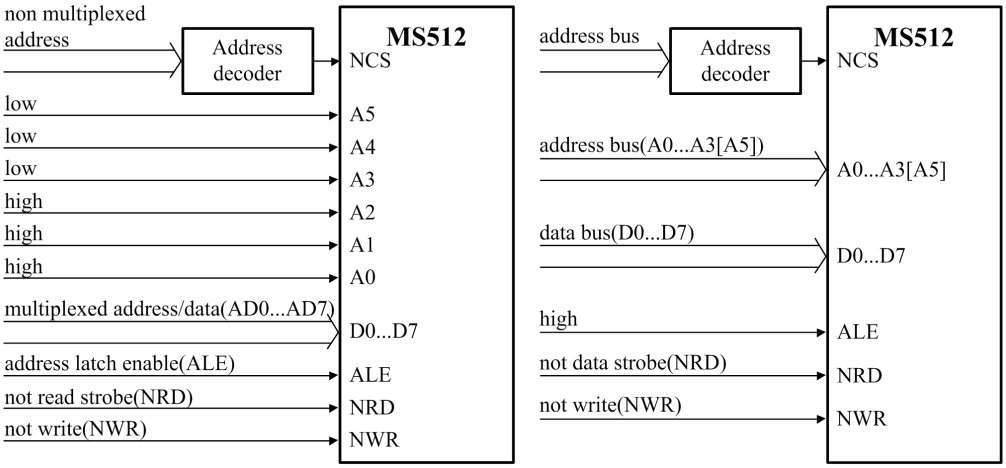


Figure 12. Connection to host controller with separated Read/Write strobes

1.6.2 Common Read/Write strobe

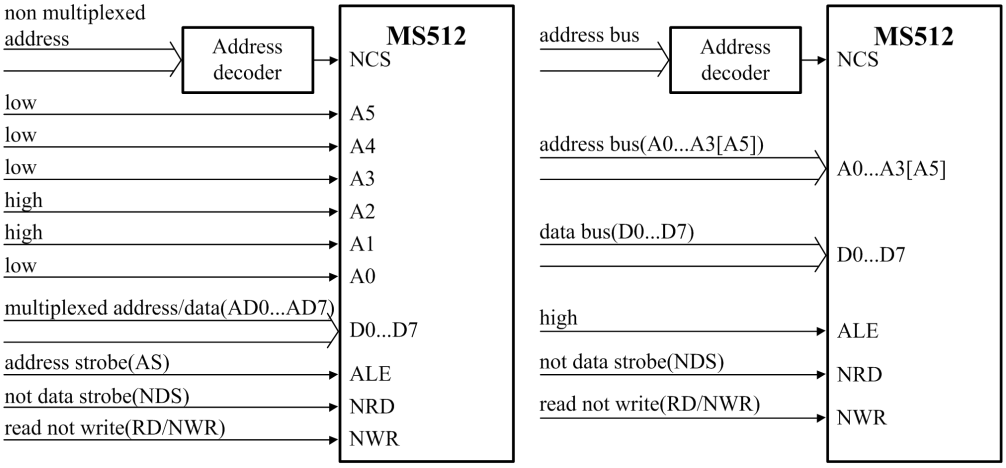


Figure 13. Connection to host controller with common Read/Write strobes

1.7 Analog interface and contactless UART

1.7.1 General

The integrated contactless UART supports the external host online with framing and error checking of the protocol requirements up to 848 kBd. An external circuit can be connected to the communication interface pins TIN and TOUT to modulate and demodulate the data.

The contactless UART manage the protocol requirements for the communication protocols in cooperation with the host. Protocol handling generates bit and byte-oriented framing. In addition, it manages error detection such as parity and CRC, based on the various supported contactless communication protocols.

The size and tuning of the antenna and the power supply voltage have an important impact on the achievable operating distance.

1.7.2 TX p-driver

The signal on pins TX1 and TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. It can be used to drive an antenna directly using a few passive components for matching and filtering.

The modulation index can be set by adjusting the impedance of the drivers. The modulation index also depends on the antenna design and tuning.

1.7.3 RF level detector

The RF level detector is integrated to fulfill NFCIP1 protocol requirements (RF collision avoidance). Furthermore the RF level detector can be used to wake up the MS512 and to generate an interrupt.

1.7.4 Serial data switch

Two main blocks are implemented in the MS512. The digital block comprises the state machines, encoder/decoder logic. The analog block comprises the modulator and antenna drivers, the receiver and amplifiers. It is possible for the interface between these two blocks to be configured so that the interfacing signals are routed to pins SIGIN and SIGOUT. This topology allows the analog block of the MS512 to be connected to the digital block of another device.

1.7.5 S^2C interface

The S^2C provides the possibility to directly connect a secure IC to the MS512 in order act as a contactless smart card IC via the MS512. The interfacing signals can be routed to the pins SIGIN and SIGOUT. SIGIN can receive either a digital FeliCa or digitized ISO/IEC 14443A signal sent by the secure IC. The SIGOUT pin can provide a digital signal and a clock to communicate to the secure IC.

Configured in the Secure Access Mode the host controller can directly communicate to the Secure IC via SIGIN/SIGOUT. In this mode the MS512 generates the RF clock and performs the communication on the SIGOUT line. To enable the Secure Access module mode the clock has to be derived by the internal oscillator of the MS512.

Configured in Contactless Card mode the secure IC can act as contactless smart card IC via the MS512. In this mode the signal on the SIGOUT line is provided by the external RF field of the external reader/writer. To enable the Contactless Card mode the clock derived by the external RF field has to be used.

1.7.5.1 Signal shape for Felica S2C interface support

The FeliCa secure IC is connected to the MS512 via the pins SIGOUT and SIGIN.The signal at SIGOUT contains the information of the 13.56 MHz clock and the digitized demodulated signal. The clock and the demodulated signal is combined by using the logical function exclusive or.

To ensure that this signal is free of spikes, the demodulated signal is digitally filtered first. The time delay for that digital filtering is in the range of one bit length. The demodulated signal changes only at a positive edge of the clock.

The answer of the FeliCa SAM is transferred from SIGIN directly to the antenna driver.

1.7.5.2 Waveform shape for ISO/IEC 14443A S2C interface support

The waveform shape at SIGOUT is a digital 13.56 MHz Miller coded signal with levels between PVSS and PVDD derived out of the external 13.56 MHz carrier signal in case of the Contactless Card mode or internally generated in terms of Secure Access mode.

The signal at SIGIN is a digital Manchester coded signal according to the requirements of the ISO/IEC 14443A with the subcarrier frequency of 847.5 kHz generated by the secure IC.

1.7.6 Hardware support for FeliCa and NFC polling

1.7.6.1 Polling sequence functionality for initiator

1. Timer: The MS512 has a timer, which can be programmed in a way that it generates an interrupt at the end of each timeslot, or if required an interrupt is generated at the end of the last timeslot.

2. The receiver can be configured in a way to receive continuously. In this mode it can receive any number of packets. The receiver is ready to receive the next packet directly after the last packet has been received.

3. The internal UART adds one byte to the end of every received packet, before it is transferred into the FIFO-buffer.

This byte indicates if the received byte packet is correct. The first byte of each packet contains the length byte of the packet.

4. The length of one packet is 18 or 20 bytes (+ 1 byte Error-Info). The FIFO has a length of 64 bytes. This means three packets can be stored in the FIFO at the same time. If more than three packets are expected, the host controller has to empty the FIFO, before the FIFO is filled completely. In case of a FIFO-overflow data is lost.

1.7.6.2 Polling sequence functionality for target

1. The host controller has to configure the MS512 with the correct polling response parameters for the polling command.

2. To activate the automatic polling in Target mode, the AutoColl Command has to be activated.

3. The MS512 receives the polling command send out by an initiator and answers with the polling response. The timeslot is selected automatically (The timeslot itself is randomly generated, but in the range 0 to TSN, which is defined by the Polling command). The MS512 compares the system code, stored in byte 17 and 18 of the Config Command with the system code received by the polling command of an initiator. If the system code is equal, the MS512 answers according to the configured polling response. The system code FFh acts as a wildcard for the system code bytes, i.e. a target of a system code 1234h answers to the polling command with one of the following system codes 1234h, 12FFh, FF34h or FFFFh. If the system code does not match no answer is sent back by the MS512.

If a valid command is received by the MS512, which is not a Polling command, no answer is sent back and the command AutoColl is stopped. The received packet is stored in the FIFO.

1.7.6.3 CRC coprocessor

The following CRC coprocessor parameters can be configured:

- The CRC preset value can be either 0000h, 6363h, A671h or FFFFh
- The CRC polynomial for the 16-bit CRC is fixed to x16 +x12 +x5 +1

Table 14. CRC coprocessor parameters

Parameter	Value
CRC register length	16-bit CRC
CRC algorithm	according to ISO/IEC 14443 A and ITU-T
CRC preset value	0000h, 6363h, A671h or FFFFh

1.8 FIFO buffer

An 8 x 64 bit FIFO buffer is used in the MS512. It buffers the input and output data stream between the host and the MS512's internal state machine. This makes it possible to manage data streams up to 64 bytes long without the need to take timing constraints into account.

1.8.1 Accessing the FIFO buffer

The FIFO buffer input and output data bus is connected to the register. Writing to register stores one byte in the FIFO buffer and increments the internal FIFO buffer write pointer. Reading from this register shows the FIFO buffer contents stored in the FIFO buffer read pointer and decrements the FIFO buffer read pointer. The distance between the write and read pointer can be obtained by reading the register.

When the microcontroller starts a command, the MS512 can, while the command is in progress, access the FIFO buffer according to that command. Only one FIFO buffer has been implemented which can be used for input and output. The microcontroller must ensure that there are not any unintentional FIFO buffer accesses.

1.8.2 Controlling the FIFO buffer

The FIFO buffer pointers can be reset by setting register. The bytes stored in the FIFO buffer are no longer accessible allowing the FIFO buffer to be filled with another 64 bytes.

1.8.3 FIFO buffer status information

The host can get the following FIFO buffer status information:

- Number of bytes stored in the FIFO buffer
- FIFO buffer almost full warning
- FIFO buffer almost empty warning
- FIFO buffer overflow warning

1.9 Timer unit

The MS512 has a timer unit which the external host can use to manage timing tasks. The timer unit can be used in one of the following timer/counter configurations:

- Timeout counter
- Watchdog counter
- Stop watch
- Programmable one shot
- Periodic trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events explained in the paragraphs below. The timer does not influence any internal events, for example, a time-out during data reception does not automatically influence the reception process. In addition, several timer-related bits can be used to generate an interrupt.

The timer has an input clock of 13.56 MHz derived from the 27.12 MHz quartz crystal oscillator. The timer consists of two stages: prescaler and counter.

1.10 Power reduction modes

1.10.1 Hard power-down mode

Hard power-down is enabled when pin NRSTPD is LOW. This turns off all internal current sinks including the oscillator. All digital input buffers are separated from the input pins and clamped internally (except pin NRSTPD). The output pins are frozen at either a HIGH or LOW level.

1.10.2 Soft power-down mode

All internal current sinks are switched off, including the oscillator buffer in soft power-down mode. However, the digital input buffers are not separated from the input pins and keep their functionality. The digital output pins do not change their state.

During soft power-down, all register values, the FIFO buffer content and the configuration keep their current contents.

1.10.3 Transmitter Power-down mode

The Transmitter Power-down mode switches off the internal antenna drivers and the RF field.

1.11 Oscillator circuit

The clock applied to the MS512 provides a time basis for the synchronous system ’ s encoder and decoder. The stability of the clock frequency is an important factor for correct operation. To obtain optimum performance, clock jitter must be reduced as much as possible. This is best achieved using the internal oscillator buffer with the

recommended circuitry.

If an external clock source is used, the clock signal must be applied to pin OSCIN. In this case, be very careful in optimizing clock duty cycle and clock jitter. Ensure the clock quality has been verified.

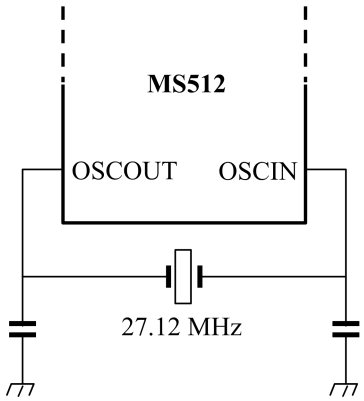


Figure 14. Quartz crystal connection

1.12 Reset and oscillator start-up time

1.12.1 Reset timing requirements

The reset signal is filtered by a hysteresis circuit and a spike filter before it enters the digital circuit. The spike filter rejects signals shorter than 10 ns. In order to perform a reset, the signal must be LOW for at least 100 ns.

1.12.2 Oscillator start-up time

If the MS512 has been set to a Power-down mode or is powered by a VDDX supply, the start-up time for the MS512 depends on the oscillator used and is shown in Figure 15.

The time (tstartup) is the start-up time of the crystal oscillator circuit. The crystal oscillator start-up time is defined by the crystal.

The time (td) is the internal delay time of the MS512 when the clock signal is stable before the MS512 can be addressed.

The delay time is calculated by:

$$td = \frac{1024}{27\ \mu s} = 37.74\mu s$$

The time (tosc) is the sum of td and tstartup.

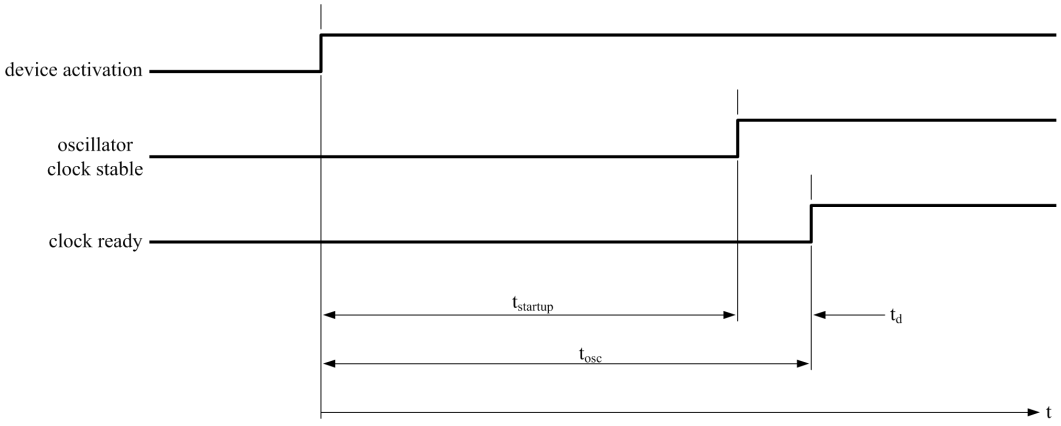
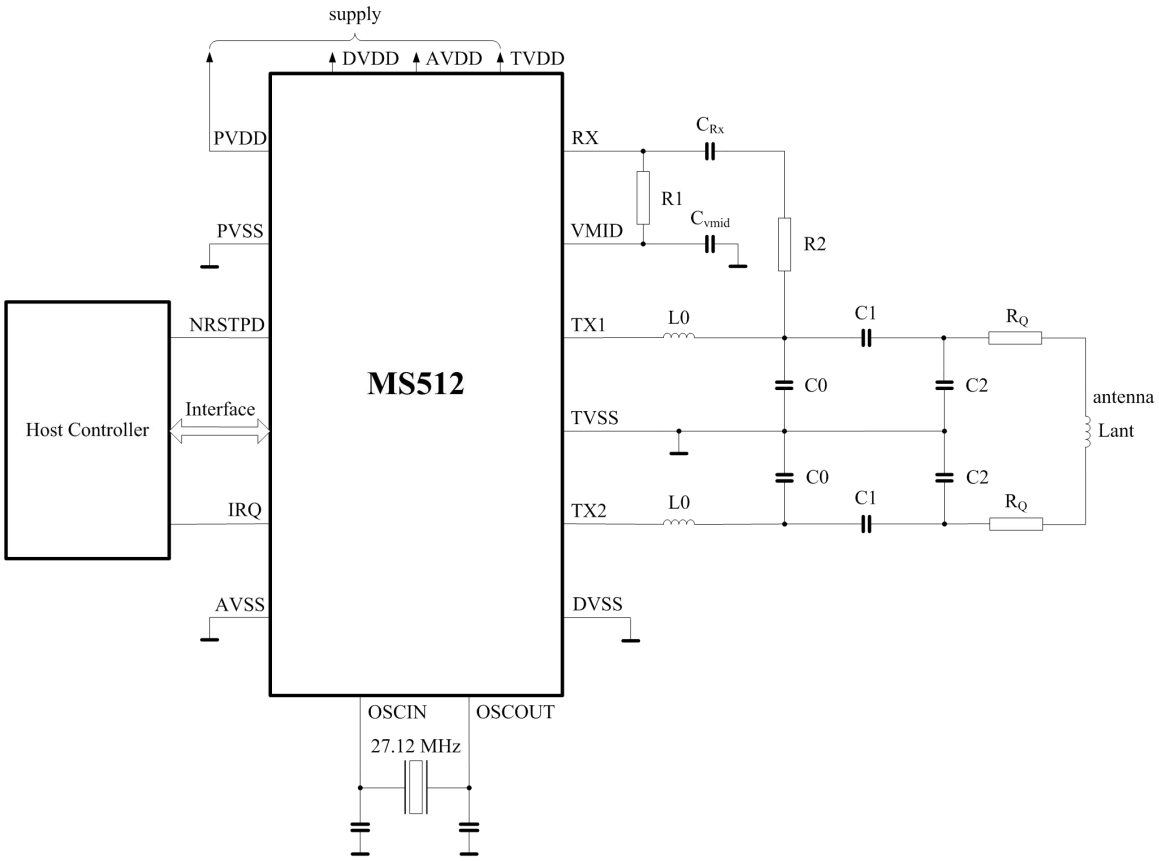


Figure 15. Oscillator start-up time

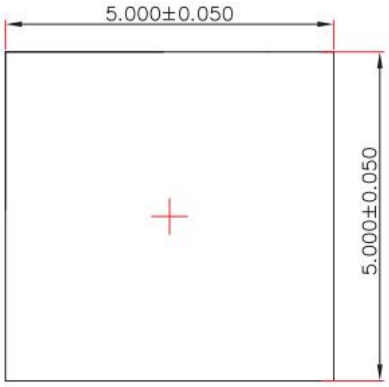
TYPICAL APPLICATION DIAGRAM

A typical application diagram using a complementary antenna connection to the MS512.

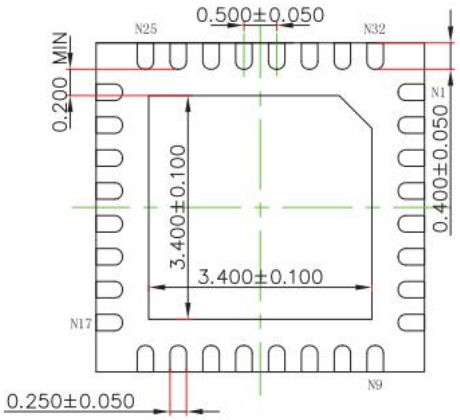


PACKAGE OUTLINE DIMENSIONS

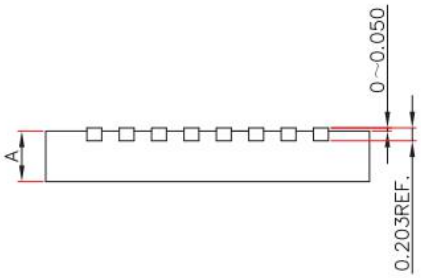
QFN32:



TOP VIEW



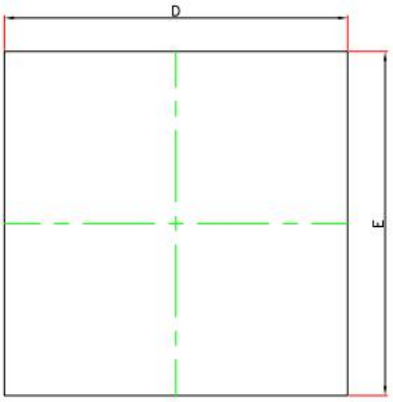
BOTTOM VIEW



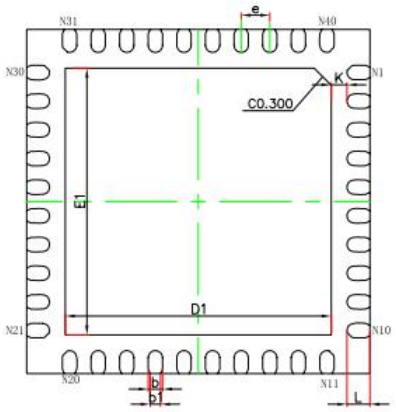
SIDE VIEW

	MIN	NOR	MAX
A	0.700	0.750	0.800

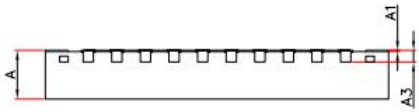
QFN40:



TOP VIEW



BOTTOM VIEW

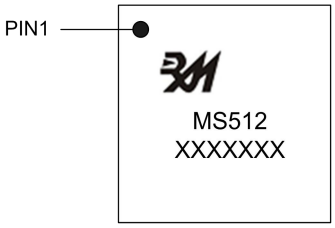


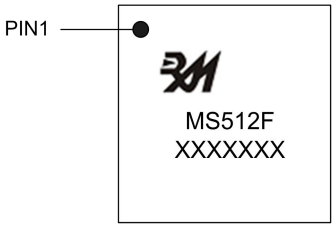
SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	5.900	6.100	0.232	0.240
E	5.900	6.100	0.232	0.240
D1	4.550	4.750	0.179	0.187
E1	4.550	4.750	0.179	0.187
b	0.200	0.300	0.008	0.012
b1	0.180REF.		0.007REF.	
e	0.500BSC.		0.020BSC.	
k	0.275REF.		0.011REF.	
L	0.300	0.500	0.012	0.020

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description





MS512、MS512F：product name

XXXXXXX：Product code

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS512	QFN32	1000	8	8000	4	32000
MS512F	QFN40	2000	1	2000	8	16000

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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