Micro-programmed Control Unit (MCU)

PRODUCT DESCRIPTION

The MS616F512 is a low dissipation, 16-bit RISC MCU. It has five low dissipation modes, which greatly increases battery lifespan of portable device . The digital oscillator could arouse CPU from low dissipation mode within 6μs.

LQFP100

FEATURES

- Low Power Supply : 1.8V-3.6V
- Ultra-low Dissipation
  Operation Status : 280μA (1MHz,2.2V)
  Standby Status：1.1μA
  Off Status (RAM hold)：0.1μA
- Five Power Saving Modes
- From Standby Mode to Wake-up Mode Within 6μs
- 16-bit RISC Architecture, 125ns Instruction Period
- 16-bit Timer A with Three Capture/Compare Registers
- 16-bit Timer B with Seven Capture/Compare Registers
- A Integrated Comparator
- Serial Communication Interface(USART)
  Optional Synchronous or Asynchronous Mode
- Low voltage Detection
- On-line Flash Programming via JTAG, BSL
- Support Onboard Programming and Erasing
- Up to 160 LCD Drive Modules
- 2KB RAM
- 62KB+128B Flash Memory

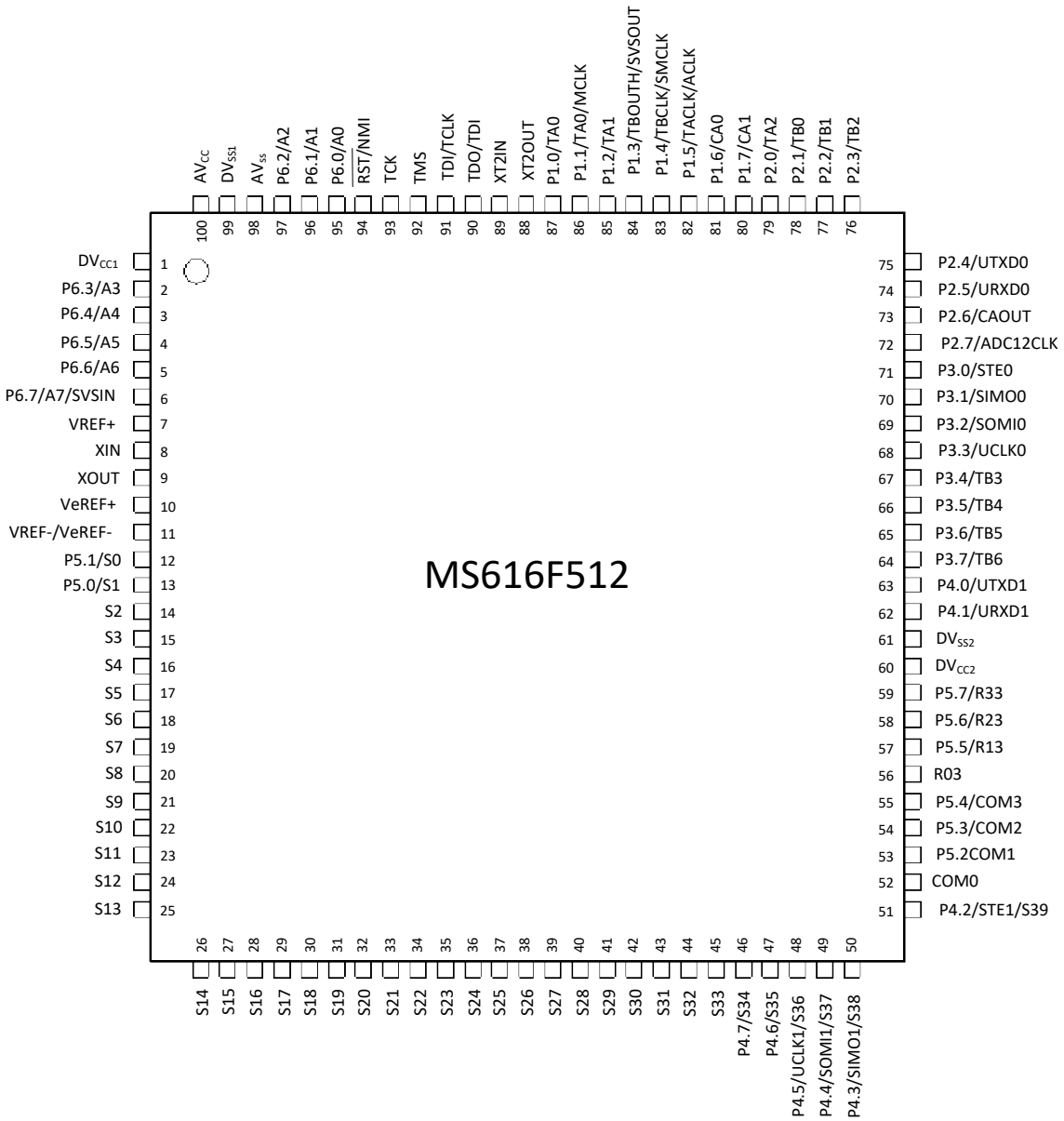
APPLICATIONS

- Measurement
- Industrial Control

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS616F512	LQFP100	MS616F512

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	DVCC1	P	Digital Power Supply, Positive Terminal
2	P6.3/A3	I/O	General Digital I/O Interface / 12-bit ADC Analog Input A3
3	P6.4/A4	I/O	General Digital I/O Interface / 12-bit ADC Analog Input A4
4	P6.5/A5	I/O	General Digital I/O Interface / 12-bit ADC Analog Input A5
5	P6.6/A6	I/O	General Digital I/O Interface / 12-bit ADC Analog Input A6
6	P6.7/A7/SVSIN	I/O	General Digital I/O Interface / 12-bit ADC Analog Input A7 / Analog Input of Supply Voltage Supervisor(SVS)
7	VREF+	O	ADC Internal Reference Voltage, Positive Output Terminal
8	XIN	I	Input Terminal of Crystal Oscillator XT1 , can connect to standard or clock crystal
9	XOUT	O	Output Terminal of Crystal Oscillator XT1
10	VeREF+	I	Input Terminal of ADC External Reference Voltage
11	VREF-/VeREF-	I	Negative Terminal of ADC Reference Voltage, including internal and external references
12	P5.1/S0	I/O	General Digital I/O Interface / LCD Segment Output 0
13	P5.0/S1	I/O	General Digital I/O Interface / LCD Segment Output 1
14	S2	O	LCD Segment Output 2
15	S3	O	LCD Segment Output 3
16	S4	O	LCD Segment Output 4
17	S5	O	LCD Segment Output 5
18	S6	O	LCD Segment Output 6
19	S7	O	LCD Segment Output 7
20	S8	O	LCD Segment Output 8
21	S9	O	LCD Segment Output 9
22	S10	O	LCD Segment Output 10
23	S11	O	LCD Segment Output 11
24	S12	O	LCD Segment Output 12
25	S13	O	LCD Segment Output 13
26	S14	O	LCD Segment Output 14
27	S15	O	LCD Segment Output 15
28	S16	O	LCD Segment Output 16
29	S17	O	LCD Segment Output 17
30	S18	O	LCD Segment Output 18

Pin	Name	Type	Description
31	S19	O	LCD Segment Output 19
32	S20	O	LCD Segment Output 20
33	S21	O	LCD Segment Output 21
34	S22	O	LCD Segment Output 22
35	S23	O	LCD Segment Output 23
36	S24	O	LCD Segment Output 24
37	S25	O	LCD Segment Output 25
38	S26	O	LCD Segment Output 26
39	S27	O	LCD Segment Output 27
40	S28	O	LCD Segment Output 28
41	S29	O	LCD Segment Output 29
42	S30	O	LCD Segment Output 30
43	S31	O	LCD Segment Output 31
44	S32	O	LCD Segment Output 32
45	S33	O	LCD Segment Output 33
46	P4.7/S34	I/O	General Digital I/O Interface / LCD Segment Output 34
47	P4.6/S35	I/O	General Digital I/O Interface / LCD Segment Output 35
48	P4.5/UCLK1/S36	I/O	General Digital I/O Interface / In SPI Mode, USART1 Master Out, Slave In / LCD Segment Output 36
49	P4.4/SOMI1/S37	I/O	General Digital I/O Interface / In SPI Mode, USART1 Master In, Slave Out / LCD Segment Output 37
50	P4.3/SIMO1/S38	I/O	General Digital I/O Interface / In SPI Mode, USART1 Master Out, Slave In / LCD Segment Output 38
51	P4.2/STE1/S39	I/O	General Digital I/O Interface / In SPI Mode, USART1 Slave Transmission Enable / LCD Segment Output 39
52	COM0	O	LCD Common Output 0
53	P5.2/COM1	I/O	General Digital I/O Interface / LCD Common Output 1
54	P5.3/COM2	I/O	General Digital I/O Interface / LCD Common Output 2
55	P5.4/COM3	I/O	General Digital I/O Interface / LCD Common Output 3
56	R03	I	LCD Analog Input Terminal 0
57	P5.5/R13	I/O	General Digital I/O Interface / LCD Analog Input Terminal 1
58	P5.6/R23	I/O	General Digital I/O Interface / LCD Analog Input Terminal 2
59	P5.7/R33	I/O	General Digital I/O Interface / LCD Analog Output Terminal
60	DVCC2	P	Digital Power Supply, Positive Terminal

Pin	Name	Type	Description
61	DVSS2	P	Digital Power Supply,Negative Terminal
62	P4.1/URXD1	I/O	General Digital I/O Interface / In UART Mode, USART1 Receiving Data Input
63	P4.0/UTXD1	I/O	General Digital I/O Interface / In UART Mode, USART1 Transmitting Data Output
64	P3.7/TB6	I/O	General Digital I/O Interface / Capture Input of Timer_B7 CCR6 : CCI6A/CCI6B, Compare Output: OUT6
65	P3.6/TB5	I/O	General Digital I/O Interface / Capture Input of Timer_B7 CCR5 : CCI5A/CCI5B, Compare Output: OUT5
66	P3.5/TB4	I/O	General Digital I/O Interface / Capture Input of Timer_B7 CCR4 : CCI4A/CCI4B, Compare Output: OUT4
67	P3.4/TB3	I/O	General Digital I/O Interface / Capture Input of Timer_B7 CCR3 : CCI3A/CCI3B, Compare Output: OUT3
68	P3.3/UCLK0	I/O	General Digital I/O Interface / In SPI Mode, USART0 Master Out, Slave In
69	P3.2/SOMI0	I/O	General Digital I/O Interface / In SPI Mode, USART0 Master In, Slave Out
70	P3.1/SIMO0	I/O	General Digital I/O Interface / In SPI Mode, USART0 Master Out, Slave In
71	P3.0/STE0	I/O	General Digital I/O Interface / In SPI Mode, USART0 Slave Transmission Enable
72	P2.7/ADC12CLK	I/O	General Digital I/O Interface / 12-bit ADC Conversion Clock
73	P2.6/CAOUT	I/O	General Digital I/O Interface / Comparator A Output
74	P2.5/URXD0	I/O	General Digital I/O Interface / In UART Mode, USART0 Receiving Data Input
75	P2.4/UTXD0	I/O	General Digital I/O Interface / In UART Mode, USART0 Transmitting Data Output
76	P2.3/TB2	I/O	General Digital I/O Interface / Capture Input of Timer_B7 CCR2 : CCI2A/CCI2B, Compare Output: OUT2
77	P2.2/TB1	I/O	General Digital I/O Interface / Capture Input of Timer_B7 CCR1 : CCI1A/CCI1B, Compare Output: OUT1
78	P2.1/TB0	I/O	General Digital I/O Interface / Capture Input of Timer_B7 CCR0 : CCI0A/CCI0B, Compare Output: OUT0
79	P2.0/TA2	I/O	General Digital I/O Interface / Capture Input of Timer_A : CCI2A , Compare Output: OUT2

Pin	Name	Type	Description
80	P1.7/CA1	I/O	General Digital I/O Interface / Comparator A Input
81	P1.6/CA0	I/O	General Digital I/O Interface / Comparator A Input
82	P1.5/TACLK/ ACLK	I/O	General Digital I/O Interface / Timer_A Clock Signal, TACLK Input / Auxiliary Clock ACLK Output
83	P1.4/TBCLK/ SMCLK	I/O	General Digital I/O Interface / Timer_B Clock Signal, TBCLK Input / Submain System SMCLK Output
84	P1.3/TBOUTH/ SVSOUT	I/O	General Digital I/O Interface / All PWM Digital Output Terminals of Timer_B (TB0-TB6) Switched to High-impedance / SVS Comparator Output
85	P1.2/TA1	I/O	General Digital I/O Interface / Capture Input of Timer_A : CCI1A , Compare Output: OUT1
86	P1.1/TA0/ MCLK	I/O	General Digital I/O Interface / Capture Input of Timer_A : CCI0B / Master Clock MCLK Output
87	P1.0/TA0	I/O	General Digital I/O Interface / Capture Input of Timer_A : CCI0A , Compare Output: OUT0
88	XT2OUT	O	Output Terminal of Crystal Oscillator XT2
89	XT2IN	I	Input Terminal of Crystal Oscillator XT2 , just can connect to standard crystal
90	TDO/TDI	I/O	Test Data Output. JTAG Data Output / JTAG Data Input
91	TDI/TCLK	I	Test Data or Clock Input. JTAG Data Input / TCLK Input. The protection fuse is connected to TDI/TCLK.
92	TMS	I	Test Mode Selection. TMS is used as input terminal for JTAG programming and test.
93	TCK	I	Test Clock. TCK is clock input terminal for JTAG programming and test.
94	RST/NMI	I	Reset Input / No-shield Interrupt Input Terminal
95	P6.0/A0	I/O	General Digital I/O Interface / 12-bit ADC Analog Input A0
96	P6.1/A1	I/O	General Digital I/O Interface / 12-bit ADC Analog Input A1
97	P6.2/A2	I/O	General Digital I/O Interface / 12-bit ADC Analog Input A2
98	AVSS	P	Analog Power Supply, Negative Terminal
99	DVSS1	P	Digital Power Supply, Negative Terminal
100	AVCC	P	Analog Power Supply, Positive Terminal

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Range	Unit
Voltage Difference From VCC to VSS	-0.3 ~ 4.1	V
Input Voltage	-0.3 ~ VDD + 0.3	V
Device Diode Current	±2	mA
Operating Temperature (No Programming)	-55 ~ +150	°C
Storage Temperature (Programming)	-40 ~ +85	°C

Note: All voltages are relative to ground. VFB, the JTAG fuse-blow voltage, could operate in maximum rating. When it needs to blow the fuse, TDI pin provides voltage.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply	VCC	Program executing	1.8		3.6	V
		Program executing and SVS enable	2.0		3.6	V
		Flash Programming	2.7		3.6	V
Power Supply	VSS		0		0	V
Operating Temperature	TA		-40		85	°C
LFXT1 Frequency	f_{LFXT1}	XTS_FLL = 0, Quartz Oscillator		32.768		kHz
		XTS_FLL = 1, Ceramic Oscillator	450		8000	kHz
		XTS_FLL = 1, Crystal Oscillator	1000		8000	kHz
XT2 Frequency	f_{XT2}	Ceramic Oscillator	450		8000	kHz
		Crystal Oscillator	1000		8000	kHz
System Clock Frequency	f_{System}	VCC = 3.6V	DC		4	MHz

1. It's recommended to use the same power supply for AVCC and DVCC. The voltage difference between AVCC and DVCC can't exceed 0.3V.

2. When the power supply enough lows to trigger POR, the corresponding voltage is the minimum operating voltage. When the power supply increases to the value, which is equal to the minimum voltage value adding to SVS hysteresis voltage, the POR signal stops.

3. In LF mode, the LFXT1 oscillator needs to connect with one external quartz oscillator. While in XT1 mode, LFXT1 needs to connect with ceramic or crystal oscillator.

ELECTRICAL CHARACTERISTICS

Supply Current

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Operation Mode (Note 1) $f_{MCLK}=f_{SMCLK}$=1MHz, f_{ACLK}=32768Hz, XTS_FLL=0, SELM=(0,1)	I_{AM}	TA=-40°C to 85°C	VCC = 2.2V		280	350	μA
			VCC = 3V		420	560	
Low Dissipation Mode (Note 1,4)	I_{LPM0}	TA=-40°C to 85°C	VCC = 2.2V		32	45	μA
			VCC = 3V		55	70	
Low Dissipation Mode (Note 2,4) $f_{MCLK}=f_{SMCLK}$=0MHz, f_{ACLK}=32768Hz, SCG=0	I_{LPM2}	TA=-40°C to 85°C	VCC = 2.2V		11	14	μA
			VCC = 3V		17	22	
Low Dissipation Mode (Note 3,4) $f_{MCLK}=f_{SMCLK}$=0MHz, f_{ACLK}=32768Hz, SCG=1	I_{LPM3}	TA=-40°C	VCC = 2.2V		1	1.5	μA
		TA=25°C			1.1	1.5	
		TA=60°C			2	3	
		TA=85°C			3.5	6	
		TA=-40°C	VCC = 3V		1.8	2.2	
		TA=25°C			1.6	1.9	
		TA=60°C			2.5	3.5	
		TA=85°C			4.2	7.5	
Low Dissipation Mode (Note 2,4) $f_{MCLK}=f_{SMCLK}$=0MHz, f_{ACLK}=0Hz, SCG=1	I_{LPM4}	TA=-40°C	VCC = 2.2V		0.1	0.5	μA
		TA=25°C			0.1	0.5	
		TA=60°C			0.7	1.1	
		TA=85°C			1.7	3	
		TA=-40°C	VCC = 3V		0.1	0.5	
		TA=25°C			0.1	0.5	
		TA=60°C			0.8	1.2	
		TA=85°C			1.9	3.5	

Note:

1. Timer_B frequency is locked as $f_{DCOCLK}=f_{DCO}$=1MHz. All inputs are connected to 0V or VCC. All outputs have no source or reverse current.

2. All inputs are connected to 0V or VCC. All outputs have no source or reverse current.

3. All inputs are connected to 0V or VCC. All outputs have no source or reverse current. The current consumed of LPM3 is achieved through measuring the operating current of timer 1 and LCD (select ACLK). Comparator A and the SVS current would be described specially.

4. Including the current consumption in BROWNOUT.

In operation mode, the relationship between consumption current and system frequency:

$$I_{(AM)} = I_{(AM)}\ [1MHZ] \times f_{(System)}\ [MHZ]$$

In operation mode, the relationship between consumption current and power supply:

$$I_{(AM)} = I_{(AM)\ [3V]} + 175\ \mu A/V \times (VCC - 3V)$$

Schmitt Trigger Input Terminal- P1, P2, P3, P4, P5, P6

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Forward Input Threshold Voltage	V_{IT+}	VCC = 2.2V	1.1		1.5	V
		VCC = 3V	1.5		1.9	V
Reverse Input Threshold Voltage	V_{IT-}	VCC = 2.2V	0.4		0.9	V
		VCC = 3V	0.9		1.3	V
Input Hysteresis(V_{IT+} - V_{IT-})	V_{hys}	VCC = 2.2V	0.3		1.1	V
		VCC = 3V	0.5		1	V

Standard Input Terminal - RST/NMI, JTAG (TCK, TMS, TDI, TDO)

Parameter	Symbol	Condition	Min	Max	Unit
Low Level Input Voltage	V_{IL}	VCC = 2.2V/3V	VSS	VSS + 0.6	V
High Level Input Voltage	V_{IH}	VCC = 2.2V/3V	0.8VCC	VCC	V

Input Terminal - Px.x, TAx, TBx

Parameter	Symbol	Condition	Min	Typ	Max	Unit
External Interrupt Timing	$t_{(int)}$	Terminal P1,P2: P1.x to P2.x, External trigger signal is interrupt flag (Note 1)	2.2/3V	1.5		Cycle
			2.2V	62		ns
			3V	50		ns
Timer_A, Timer_B Capture Time	$t_{(cap)}$	TA0,TA1,TA2,TB0,TB1,TB2,TB3 ,TB4,TB5,TB6	2.2V	62		ns
			3V	62		ns
Clock Frequency added to Timer_A/B	$f_{(TAext)}$	TACLK, TBCLK, INCLK: $t_{(H)}$=$t_{(L)}$	2.2V		8	MHz
	$f_{(TBext)}$		3V		10	MHz
Clock Frequency of Timer_A/B	$f_{(TAint)}$	Select SMCLK or ACLK	2.2V		8	MHz
	$f_{(TBint)}$		3V		10	MHz

Note 1: When the external signal sets the interrupt flag, the corresponding $t_{(int)}$ is even with trigger signal shorter than $t_{(int)}$. The clock period and time parameter must be met simultaneously to ensure interrupt flag setting. $t_{(int}$ is measured referring MCLK period.

Leakage Current (Note 1,2)

Parameter	Symbol	Condition	VCC	Min	Max	Unit
Px.x Leakage Current	I_{lkg}	Px： $V_{(Px.x)}$	2.2/3V		50	nA

Note :

1. Leakage current is measured when VSS or VCC is added to relative pins. Unless otherwise noted.
2. The terminal pin must be set as input , and couldn't have any pullup or pulldown resistor.

Output Terminal- P1,P2,P3,P4,P5,P6

Parameter	Symbol	Condition	Min	Max	Unit
High Level Output Voltage	V_{OH}	$I_{OH(max)}$ = -1.5mA, VCC = 2.2V (Note 1)	VCC - 0.25	VCC	V
		$I_{OH(max)}$ = -6mA, VCC = 2.2V (Note 2)	VCC - 0.6	VCC	V
		$I_{OH(max)}$ = -1.5mA, VCC = 3V (Note 1)	VCC - 0.25	VCC	V
		$I_{OH(max)}$ = -6mA, VCC = 3V (Note 2)	VCC - 0.6	VCC	V
Low Level Output Voltage	V_{OL}	$I_{OL(max)}$ = 1.5mA, VCC = 2.2V (Note 1)	VSS	VSS + 0.25	V
		$I_{OL(max)}$ = 6mA, VCC = 2.2V (Note 2)	VSS	VSS + 0.6	V
		$I_{OL(max)}$ = 1.5mA, VCC = 3V (Note 1)	VSS	VSS + 0.25	V
		$I_{OL(max)}$ = 6mA, VCC = 3V (Note 2)	VSS	VSS + 0.6	V

Note :

1. $I_{OH(max)}$ and $I_{OL(max)}$ is the maximum total current, sum of all output currents. Only when it is less than 12mA, just meet maximum voltage without drop.
2. $I_{OH(max)}$ and $I_{OL(max)}$ is the maximum total current, sum of all output currents. Only when it is less than 48mA, just meet maximum voltage without drop.

Output Frequency

Parameter	Condition		Min	Typ	Max	Unit
f(Px.y) (1≤x≤6,0≤x≤7)	C_L = 20pF, I_L = 1.5mA	VCC = 2.2V	DC		5	MHz
		VCC = 3V	DC		7.5	MHz
f(ACLK)	C_L = 20pF				$f_{(System)}$	MHz
f(MCLK)						
f(SMCLK)						
Output Duty Cycle $t_{(Xdc)}$	P1.5/TACLK/ACLK, C_L = 20 pF, VCC = 2.2 V / 3 V	$f_{(ACLK)} = f_{(LFXT1)} = f_{(XT1)}$	40		60	
		$f_{(ACLK)} = f_{(LFXT1)} = f_{(LF)}$	30		70	
		$f_{(ACLK)} = f_{(LFXT1)}$		50		
	P1.1/TA0/MCLK, C_L = 20 pF, VCC = 2.2 V / 3 V	$f_{(MCLK)} = f_{(XT1)}$	40		60	
		$f_{(MCLK)} = f_{(DCOCLK)}$	50%-15ns	50%	50%+15ns	
Output Duty Cycle $t_{(Xdc)}$	P1.4/TBCLK/SMCLK, C_L = 20 pF, VCC = 2.2 V / 3 V	$f_{(SMCLK)} = f_{(XT2)}$	40		60	
		$f_{(SMCLK)} = f_{(DCOCLK)}$	50%-15ns	50%	50%+15ns	

Wake-up LPM3

Parameter	Condition		Min	Typ	Max	Unit
Delay Time $t_{d(LPM3)}$	f = 1MHz	VCC = 2.2V/3V			6	μs
	f = 2MHz				6	μs
	f = 3MHz				6	μs

RAM

Parameter	Condition	Min	Typ	Max	Unit
VRAMh	CPU Stop (Note 1)	1.6			V

Note 1: The parameter defines the minimum power supply when RAM changes. And all programme must stop when measuring the parameter.

LCD

Parameter		Condition		Min	Typ	Max	Unit
Analog Voltage	$V_{(33)}$	Voltage on P5.7/R33	VCC=3V	2.5		VCC+0.2	V
	$V_{(23)}$	Voltage on P5.6/R23			$[V_{(33)}-V_{(03)}] \times 2/3 + V_{(03)}$		V
	$V_{(13)}$	Voltage on P5.5/R13			$[V_{(33)}-V_{(03)}] \times 2/3 + V_{(03)}$		V
	$V_{(33)}$-$V_{(03)}$	Voltage on R33 to R03		2.2		VCC+0.2	V
Input Leakage Current	$I_{(R03)}$	R03=VSS	There are no loads on all control and common terminals, VCC=3V			20	nA
	$I_{(R13)}$	P5.5/R13=VCC/3				20	nA
	$I_{(R23)}$	P5.6/R23=2VCC/3				20	nA
Segment Address Line Voltage	$V_{(Sxx0)}$	I(Sxx) = -3μA，VCC=3V		$V_{(03)}$		$V_{(03)}$-0.1	V
	$V_{(Sxx1)}$			$V_{(13)}$		$V_{(13)}$-0.1	V
	$V_{(Sxx2)}$			$V_{(23)}$		$V_{(23)}$-0.1	V
	$V_{(Sxx3)}$			$V_{(33)}$		$V_{(33)}$-0.1	V

Comparator A (Note 1)

Parameter		Condition		Min	Typ	Max	Unit
$I_{(CC)}$		CAON=1, CARSEL=0, CAREF=0	VCC=2.2V		25	40	μA
			VCC=3V		45	60	μA
$I_{(Refladder/RefDiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, P1.6/CA0 and P1.7/CA1 no loads	VCC=2.2V		30	50	μA
			VCC=3V		45	71	μA
$V_{(Ref025)}$		PCA0=1, CARSEL=1, CAREF=1, P1.6/CA0 and P1.7/CA1 no loads	VCC=2.2V/3V	0.23	0.24	0.25	
$V_{(Ref050)}$		PCA0=1, CARSEL=1, CAREF=2, P1.6/CA0 and P1.7/CA1 no loads	VCC=2.2V/3V	0.47	0.48	0.5	
$V_{(RefVT)}$		PCA0=1, CARSEL=1, CAREF=3, P1.6/CA0 and P1.7/CA1 no loads; TA=85°C	VCC=2.2V	390	480	540	mV
			VCC=3V	400	490	550	mV
Common-mode Input Voltage	V_{IC}	CAON=1	VCC=2.2V/3V	0		VCC - 1	V
Offset Voltage	$V_P - V_S$	Note 2	VCC=2.2V/3V	-30		30	mV
V_{hys}		CAON=1	VCC=2.2V/3V	0	0.7	1.4	mV
$t_{(response\ LH)}$		TA=25°C, overdrive voltage 10mV, no capacitor; CAF=0	VCC=2.2V	160	210	300	ns
			VCC=3V	80	150	240	ns
		TA=25°C, overdrive voltage 10mV, with capacitor; CAF=1	VCC=2.2V	1.4	1.9	3.4	μA
			VCC=3V	0.9	1.5	2.6	μA
$t_{(response\ HL)}$		TA=25°C, overdrive voltage 10mV, no capacitor; CAF=0	VCC=2.2V	130	210	300	ns
			VCC=3V	80	150	240	ns
		TA=25°C, overdrive voltage 10mV, with capacitor; CAF=1	VCC=2.2V	1.4	1.9	3.4	μA
			VCC=3V	0.9	1.5	2.6	μA

Note:

1. The leakage current of comparator A has been defined in $I_{lkg(Px.x)}$.

2. Through setting CAEX bit, make the comparator A input reverse. And measure twice continuously, the input offset voltage could be cancelled, then add the two measurements.

POR/Brownout Reset(BOR) (Note 1)

Parameter		Condition	Min	Typ	Max	Unit
$t_{d(BOR)}$	Brownout (Note 2)				2000	μs
$V_{CC(start)}$		dVCC/dt ≤ 3 V/s		$0.7V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		dVCC/dt ≤ 3 V/s			1.71	V
$V_{hys(B\_IT-)}$		dVCC/dt ≤ 3 V/s	70	130	180	mV
$t_{(reset)}$		The pulse width required by internal reset on RST/NMI pin, VCC = 2.2 V/3 V	2			μs

Note:

1. The current that consumed in Brownout module has been included in total currents ICC. The voltage range is : $V_{(B\_IT-)}$ +$V_{hys(B\_IT-)}$≤1.8V.

2. After VCC=$V_{(B\_IT-)}$ + $V_{hys(B\_IT-)}$, CPU starts to execute program after one $t_{d(BOR)}$ period. Before VCC≥VCC(min), FFL+ setting can't change. VCC(min) is the minimum power supply at operating frequency.

Supply Voltage Supervision(SVS)

Parameter	Condition		Min	Typ	Max	Unit
$t_{(SVSR)}$	dVCC/dt > 30 V/ms		5		150	μs
	dVCC/dt ≤ 30 V/ms				2000	μs
$t_{d(SVSon)}$	SVSon, VLD=0 to VLD ≠ 0, VCC = 3 V		20		150	μs
t_{settle}	VLD ≠ 0 (Note 2)				12	μs
$V_{(SVSstart)}$	VLD ≠ 0, VCC/dt ≤ 3 V/s			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	VCC/dt ≤ 3 V/s	VLD=1	70	120	155	mV
		VLD=2-14	0.004 x $V_{(SVS\_IT-)}$		0.008 x $V_{(SVS\_IT-)}$	
	VCC/dt ≤ 3 V/s, external voltage applied to A7 terminal	VLD=15	4.4		10.4	mV
$V_{(SVS\_IT-)}$	VCC /dt ≤ 3 V/s	VLD=1	1.8	1.6	2.05	V
		VLD=2	1.94	2.1	2.25	V
		VLD=3	2.05	2.2	2.37	V
		VLD=4	2.14	2.3	2.48	V
		VLD=5	2.24	2.4	2.6	V

Parameter	Condition		Min	Typ	Max	Unit
$V_{(SVS\_IT-)}$	VCC /dt ≤ 3 V/s	VLD=6	2.33	2.5	2.71	V
		VLD=7	2.46	2.65	2.86	V
		VLD=8	2.58	2.8	3	V
		VLD=9	2.69	2.9	3.13	V
		VLD=10	2.83	3.05	3.29	V
		VLD=11	2.94	3.2	3.42	V
		VLD=12	3.11	3.35	3.61	V
		VLD=13	3.24	3.5	3.76	V
		VLD=14	3.43	3.7	3.99	V
	VCC/dt ≤ 3 V/s, external voltage applied to A7 terminal	VLD=15	1.1	1.2	1.3	V
$I_{CC(SVS)}$ (Note 3)	VLD ≠ 0, VCC = 2.2 V/3 V			10	15	μA

Note:

1. The maximum operating voltage is 3.6V.

2. t_{settle} is the setting time that comparator needs to stabilize level when VLD switches from not 0 to the value between 2 and 15. The overdrive voltage is assumed to be more than 50mV.

3. The consumption current of SVS module has been included in I_{CC}.

DCO

Parameter	Condition		Min	Typ	Max	Unit
$f_{(DCOCLK)}$	N(DCO)=01Eh, FN_8=FN_4=FN_3=FN_2=0,D=2; DCOPLUS = 1, $f_{Crystal}$=32.768kHz	VCC = 2.2 V/3V		1		MHz
$f_{(DCO=2)}$	FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1	VCC = 2.2 V	0.3	0.65	1.25	MHz
		VCC = 3 V	0.3	0.7	1.3	MHz
$f_{(DCO=2)}$	FN_8=FN_4=FN_3=0， FN_2=1; DCOPLUS = 1	VCC = 2.2 V	0.7	1.3	2.3	MHz
		VCC = 3 V	0.8	1.5	2.5	MHz
$f_{(DCO=2)}$	FN_8=FN_4=0,FN_3=1,FN_2=x; DCOPLUS = 1	VCC = 2.2 V	1.2	2	3	MHz
		VCC = 3 V	1.3	2.2	3.5	MHz
S_n	$S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	N(DCO) =01Eh, FN_8=FN_4=FN_3=FN_2=0, D= 2; DCOPLUS = 0	VCC = 2.2 V	-0.2	-0.3	-0.4	%/°C
		VCC = 3 V	-0.2	-0.3	-0.4	%/°C
D_V	N(DCO) =01Eh, FN_8=FN_4=FN_3=FN_2=0, D= 2; DCOPLUS = 0	VCC = 2.2 V/3V	0	5	15	%/V

Crystal Oscillator, LFXT1 Oscillator (Note 1, 2)

Parameter		Condition	Min	Typ	Max	Unit
Integrated Input Capacitance	C_{XIN}	OSCCAPx = 0h, VCC = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, VCC = 2.2 V / 3 V		10		pF
		OSCCAPx = 2h, VCC = 2.2 V / 3 V		14		pF
		OSCCAPx = 3h, VCC = 2.2 V / 3 V		18		pF
Integrated Output Capacitance	C_{XOUT}	OSCCAPx = 0h, VCC = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, VCC = 2.2 V / 3 V		10		pF
		OSCCAPx = 2h, VCC = 2.2 V / 3 V		14		pF
		OSCCAPx = 3h, VCC = 2.2 V / 3 V		18		pF
Input Logic on XIN	V_{IL}	VCC = 2.2 V / 3 V (Note 3)	VSS		0.2VCC	V
	V_{IH}		0.8VCC		VCC	V

Note:

1. The parasitic capacitance generated from package and board is about 2pF. The crystal effective load capacitance is (C_{XIN} x C_{XOUT}) / (C_{XIN} + C_{XOUT}), which has nothing with XTS_FLL.
2. There are following principles to be observed, in order to improve the EMI characteristic of low dissipation LFXT1 oscillator, especially in LF mode(32kHz).

(1) The traces between the MS616F512 and crystal should be as short as possible.

(2) Optimal design of ground plane near oscillator pin.

(3) Avoid that other clock and data lines have crosstalk with XIN and XOUT pins.

(4) Avoid layout traces below or near XIN and XOUT pins.

(5) Through using match materials and repeated practices to reduce parasitic capacitance of XIN, XOUT pins.

(6) If use protection coating, pay attention not to cause capacitive and resistive leakage among oscillator pins.

3. Only valid when using external logic clock and must set XTS_FLL bit. While invalid when using crystal and resonator.
4. For accurate real time clock application, OSCCAPx=0h, apply recommended capacitance.

Crystal Oscillator, XT2 Oscillator (Note 1)

Parameter		Condition	Min	Typ	Max	Unit
Integrated Input Capacitance	C_{XT2IN}	OSCCAPx = 0h, VCC = 2.2 V /3 V		2		pF
Integrated Output Capacitance	C_{XT2OUT}	VCC = 2.2 V / 3 V		2		pF
Input Logic on XT2IN	V_{IL}	VCC = 2.2 V / 3 V (Note 2)	VSS		0.2VCC	V
	V_{IH}		0.8VCC		VCC	V

Note: 1. The two terminals of oscillator all need to connect with load capacitance. The accurate capacitance value is provided by crystal manufacturer.

2. Only valid when using external logic clock and must set XTS_FLL bit. While invalid when using crystal and resonator.

UASRT0,USART1 (Note 1)

Parameter		Condition	Min	Typ	Max	Unit
USART0/1 Deglitch Time	$t_{(\tau)}$	VCC = 2.2 V, SYNC = 0, UART mode	200	430	800	ns
		VCC = 3 V, SYNC = 0, UART mode	150	280	500	ns

Note 1: The signal applied to USART0/1 receiving terminal should meet the $t_{(\tau)}$ timing requirement, thus ensure URXS trigger is set. URXS trigger is set by low level pulse, which satisfies $t_{(\tau)}$ minimum timing requirement. The operating conditions set by flag bit must be independent of the timing constraint. The deglitch circuit only operate when URXD0/1 line transmit negatively.

12-bit ADC, Power Supply and Input Range Condition (Note 1)

Parameter		Condition	VCC	Min	Typ	Max	Unit
Analog Power Supply	AVCC	AVCC and DVC is connected together. VSS and DVSS is connected together. $V_{(AVSS)}=V_{(DVSS)}=0V$		2.2		3.6	V
Analog Input Voltage (Note 2)	$V_{(P6.x/Ax)}$	Applicable to all P6.0/A0 to P6.7/A7 terminals. Analog input terminal is selected by ADC12MCTLx, and P6Sel.x=1，$0 \le x \le 7$; $V_{(AVSS)} \le VP6.x/Ax \le V_{(AVCC)}$		0		V_{AVCC}	V
Operating Current on AVCC(Note 3)	I_{ADC12}	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 1, REFON = 0 SHT0=0, SHT1=0, ADC12DIV=0	2.2V		0.65	1.3	mA
			3V		0.8	1.6	mA
Operating Current on AVCC (Note 4)	I_{REF+}	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, REF2_5V = 1	3V		0.5	0.8	mA
		$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2V		0.5	0.8	mA
			3V		0.5	0.8	mA
Input Capacitance	C_I	Choose one terminal one time, P6.x/Ax	2.2V			40	pF
Input Multiplexer Resistance	R_I	$0V \le V_{Ax} \le V_{AVCC}$	3V			2000	Ω

Note :

1. Leakage current has been defined in P6.x/Ax terminal parameter sheet.
2. Analog input voltage range should be within reference voltage range, thus achieve valid conversion result.
3. Reference voltage current is not included in I_{ADC12}.
4. AVCC provides current for reference voltage module. The current is independent of ADC12ON, until conversion starts. Before A/D conversion, set REFON bit to enable built-in reference voltage module.

12-bit ADC, External Reference (Note 1)

Parameter		Condition	VCC	Min	Typ	Max	Unit
Positive External Reference Voltage Input	V_{eREF+}	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (Note 2)		1.4		VAVCC	V
Negative External Reference Voltage Input	V_{REF-}/V_{eREF-}	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (Note 3)		0		1.2	V
External Reference Differential Voltage Input	(V_{eREF+} - V_{REF-}/V_{eREF-})	$V_{eREF+} > V_{REF-}/V_{eREF-}$		1.4		VAVCC	V
Static Input Current	I_{VeREF+}	0V ≤ V_{eREF+} ≤ VAVCC	2.2V/3V			±1	μA
Static Input Current	$I_{VREF-/VeREF-}$	0V ≤ V_{eREF+} ≤ VAVCC	2.2V/3V			±1	μA

Note :

1. External reference charges and discharge capacitance array during conversion. For external reference, input capacitance C_I is dynamic load during conversion period. The dynamic impedance of reference voltage should be matched with analog source impedance recommendation, thus achieving 12-bit setting accuracy on charging.
2. The accuracy constrains the minimum of positive external reference voltage. Decreasing accuracy demand could use lower reference voltage.
3. The accuracy constrains the maximum of negative external reference voltage. Decreasing accuracy demand could use higher reference voltage.
4. The accuracy constrains the difference of external reference voltage. Decreasing accuracy demand could use lower difference reference voltage.

12-bit ADC, Built-in Reference

Parameter		Condition	VCC	Min	Typ	Max	Unit
Positive Built-in Reference Voltage	V_{REF+}	REF2_5V = 1, $I_{VREF+} \le I_{VREF+}$max	3V	2.4	2.5	2.6	V
		REF2_5V = 0, $I_{VREF+} \le I_{VREF+}$max	2.2V/3V	1.44	1.5	1.56	V
Minimum Power Supply of Positive Built-in Reference Voltage	$AVCC_{(min)}$	REF2_5V = 0, $I_{VREF+} \le$ 1mA		2.2			V
		REF2_5V = 1, $I_{VREF+} \le$ 0.5mA		V_{REF+}+0.15			V
		REF2_5V = 1, $I_{VREF+} \le$ 1mA		V_{REF+}+0.15			V
Load Current on V_{REF+}	I_{VREF+}		2.2V	0.01		-0.5	mA
			3V			-1	mA
Load Modulation Current on V_{REF+}	$I_{L(VREF)+}$	I_{VREF+} = 500μA ± 100 μA, Analog input voltage~0.75 V; REF2_5V = 0	2.2V			±2	LSB
			3V			±2	LSB

Parameter		Condition	VCC	Min	Typ	Max	Unit
Load Modulation Current on V_{REF+}	$I_{L(VREF)+}$	I_{VREF+} = 500 µA ± 100 µA, Analog input voltage ~1.25 V; REF2_5V = 1	3V			±2	LSB
Load Modulation Time on V_{REF+}	$I_{DL(VREF)+}$	I_{VREF+} = 100 µA → 900 µA, C_{VREF+} = 5 µF, Ax ~ 05V_{REF+} 1 Conversion result error ≤ 1LSB	3V			20	ns
External Capacitance on V_{REF+} (Note 1)	C_{VREF+}	REFON =1, 0 mA ≤ I_{VREF+} ≤ I_{VREF+}max	2.2V/3V	5	10		µF
Temperature Coefficient of Built-in Reference	T_{REF+}	I_{VREF+} is a constant, range: 0 mA ≤ I_{VREF+} ≤ 1 mA	2.2V/3V			+100	ppm /°C
Setting Time of Built-in Reference (Note 2)	t_{REFON}	I_{VREF+} = 0.5 mA, C_{VREF+} = 10µF, V_{REF+} = 1.5 V	2.2V			17	ms

Note :

1. Internal buffer magnifier and accuracy demand need one external capacitor. All INL and DNL tests connect two capacitors between VREF+ and AVSS, VREF-/VeREF- and AVSS.

2. Condition: the conversion error is less than ±0.5 LSB after t_{REFON} opens. The setting time is up to external capacitance load.

12-bit ADC, Timing Parameter

Parameter		Condition	VCC	Min	Typ	Max	Unit
	$f_{ADC12CLK}$	Ensure accuracy of ADC linearity parameter	2.2V/3V	0.45	5	6.3	MHz
Internal ADC12 Oscillator	$f_{ADC12OSC}$	ADC12DIV=0, $f_{ADC12CLK}$=$f_{ADC12OSC}$	2.2V/3V	3.7		6.3	MHz
Conversion	$t_{CONVERT}$	C_{VREF+} ≥ 5 µF, internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz - 6.3 MHz	2.2V/3V	2.06		3.51	ns
		External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK; ADC12SSEL ≠ 0					µs
ADC Enable Time	$t_{ADC12ON}$	(Note 1)				100	ns
Sampling Time	t_{Sample}	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, τ = [R_S + R_I] x C_I (Note 2)	3V	1220			ns
			2.2V	1400			ns

Note :

1. After ADC12ON is enable, $t_{ADC12ON}$ is the time when the conversion error is less than ±0.5 LSB.And the reference voltage and input signal have be set.

2. After about 10τ, the conversion error is less than ±0.5 LSB, t_{Sample} = ln(2n+1) x (R_S + R_I) x C_I+ 800 ns (n=12, ADC resolution , R_S= input resistance).

12-bit ADC, Linearity Parameter

Parameter		Condition	VCC	Min	Typ	Max	Unit
Integral Nonlinearity Error	E_I	1.4 V ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}) min ≤ 1.6 V	2.2V/3V			±2	LSB
		1.6 V < (V_{eREF+} – V_{REF-}/V_{eREF-}) min ≤ [$V_{(AVCC)}$]				±1.7	LSB
Differential Nonlinearity Error	E_D	(V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-})	2.2V/3V			±1	LSB
Offset Error	E_O	(V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-})	2.2V/3V		±2	±4	LSB
Gain Error	E_G	(V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-})	2.2V/3V		±1.1	±2	LSB
Total Unadjusted Error	E_T	(V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-})	2.2V/3V		±2	±5	LSB

12-bit ADC, V_{MID} Temperature Sensor and Built-in Mid-voltage V_{MID}

Parameter		Condition	VCC	Min	Typ	Max	Unit
Current on AVCC (Note 1)	I_{SENSOR}	REFON = 0, INCH = 0Ah, ADC12ON=NA, TA = 25°C	2.2V		40	120	μA
			3V		60	160	μA
	V_{SENSOR}	ADC12ON=1, INCH = 0Ah, TA = 0°C	2.2V		986	986±5%	mV
			3V		986	986±5%	mV
	TC_{SENSOR}	ADC12ON=1, INCH = 0Ah	2.2V		3.55	3.55±3%	mV/°C
			3V		3.55	3.55±3%	mV/°C
Sampling Time Required by Choosing Channel 10 (Note 2)	t_{SENSOR} (sample)	ADC12ON=1, INCH = 0Ah Conversion error ≤ 1 LSB	2.2V	30			μs
			3V	30			μs
Current Divided on Channel 11	I_{VMID}	ADC12ON=1, INCH = 0Bh (Note 3)	2.2V			NA	μA
			3V			NA	μA
Voltage Divided on Channel 11	V_{MID}	ADC12ON=1, INCH = 0Bh V_{MID} ~ 0.5V_{AVCC}	2.2V		1.1	1.1±0.04	V
			3V		1.5	1.5±0.04	V
Sampling Time Required by Choosing Channel 11	t_{VMID} (sample)	ADC12ON=1, INCH = 0Bh Conversion error ≤ 1 LSB	2.2V	1400			ns
			3V	1220			ns

Note :

1. If (ADC12ON=1, REFON=1) or (ADC12ON=1, INCH=0Ah and sampling signal at high), sensor current I_{SENSOR} would be generated. The current includes the values through senor and reference.
2. The typical equivalent impedance of the sensor is 51kΩ. The sampling time includes sensor enable time.
3. V_{MID} is used during the sampling process, without generating extra current.
4. The sampling time has included enable time, without extra time.

Flash

Parameter		Condition	VCC	Min	Typ	Max	Unit
Operating Voltage at Programming, Erasing	$V_{CC(PGM/ERASE)}$			2.7		3.6	V
The Frequency for Flash Programming Timing	f_{FTGP}			257		476	kHz
The Frequency for Flash Erasing Timing	f_{FTGE}			15		100	kHz
Current on DVCC at Programming	I_{PGM}		2.7V/3.6V		3	5	mA
Current on DVCC at Erasing	I_{ERASE}		2.7V/3.6V		3	7	mA
Accumulated Programming Time	t_{CPT}	(Note 1)	2.7V/3.6V			10	ms
Accumulated Large-scale Erasing Time	$t_{CMErase}$	(Note 2)	2.7V/3.6V	200			ms
Programming/ Erasing Duration				10^4	10^5		Cycle
Data Saving Period	$t_{Retention}$	T_J = 25°C		100			Year
Word Programming Time	t_{Word}	(Note 3)			35		t_{FTG}
Block Programming Time of the First Word	$t_{Block, 0}$				30		t_{FTG}
Block Programming Time of Each Additional Word	$t_{Block, 1-63}$				21		t_{FTG}
Waiting Time for Block Programming Finishing Sequencing	$t_{Block, End}$				6		t_{FTG}
Large-scale Erasing Time	$t_{Mass\ Erase}$				5297		t_{FTG}
Segment Erasing Time	$t_{Seg\ Erase}$				4819		t_{FTG}

Note：

1. When a 64-bit Flash module is written, it couldn't exceed accumulated programming time.The parameter is applicable to all Flash programming methods.
2. The large-scale erasing time is up to Flash timing.
   At least 11.1ms (= 5297x1/f_{FTG}, maximum = 5297x1/476kHz).
3. These values have been fixed into the state machine of Flash controller.
4. The erasing frequency on chip is less than 100K.
5. Program on chip by word format, rather than byte format.
6. Information storage only has A segment (128 bytes), without B segment.
7. 2048 bytes rather than 512 bytes in each segment of master storage.

JTAG, Interface

Parameter		Condition	VCC	Min	Typ	Max	Unit
TCK Input Frequency	f_{TCK}	(Note 1)	2.2V	0		5	MHz
			3V	0		10	MHz
Internal Pullup Resistors on TMS, TCK, TDI/TCLK	$R_{Internal}$	(Note 2)	2.2/3V	25	60	90	kΩ

Note :

1. f_{TCK} may be constrained by the timing requirement of selected module.
2. TMS, TDI/TCLK and TCK pullup resistors have been integrated.

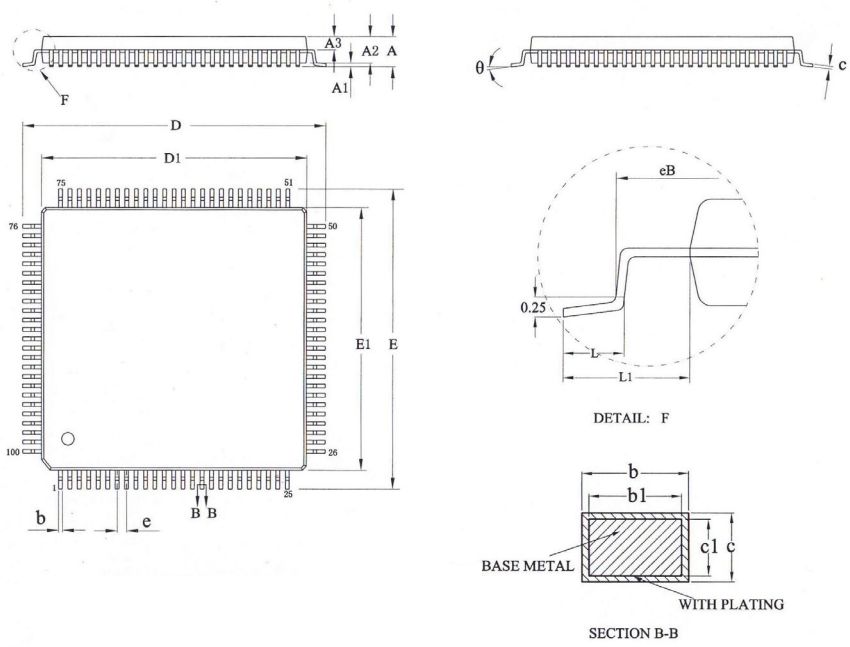
JTAG, Fuse (Note 1)

Parameter		Condition	Min	Typ	Max	Unit
Power Supply Needed by Fuse-blow	$V_{CC(FB)}$	TA = 25°C	2.5			V
TDI/TCLK Voltage Needed by Fuse-blow	V_{FB}		6		7	V
TDI/TCLK Current Needed by Fuse-blow	I_{FB}				100	mA
Time for Fuse-blow	t_{FB}				1	ms

Note 1: Once the fuse is blown, the JTAG/Test of the MS616F512 can't be connected, and the simulation characteristic would be lost. JTAG mode is switched to bypass mode.

PACKAGE OUTLINE DIMENSIONS

LQFP100



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18		0.26
b1	0.17	0.20	0.23
c	0.13		0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05		15.35
e	0.50BSC		
L	0.45		0.75
L1	1.00REF		
θ	0		7°

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description

Product Name： MS616F512

Product Code： XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Tray	Tray/Box	Piece /Box	Box/Carton	Piece/Carton
MS616F512	LQFP100	90	10	900	6	5400

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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