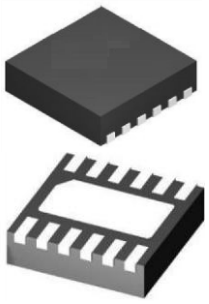
# 2.7V to 5.5V, 12Bit Quadruple DAC

## PRODUCT DESCRIPTION

The MS5224D is a 12bit, four-channel output voltage DAC. The interface uses the three-wire serial port mode, and it can be compatible with TMS320, SPI, QSPI and Microwire serial port. The MS5224D has 16bit control data, including control byte and 12bit DAC data. The power supply range is 2.7V to 5.5V. The output of integrated resistor string is connected to a class AB, rail-to-rail output amplifier with 6dB gain. The output buffer improves the stability and reduces the setup time.

The MS5224D is available in DFN12 package.



**DFN12**

## FEATURES

- 12bit Resolution
- Programmable Setup Time : 3μs or 9μs
- Compatible with TMS320,SPI and Microwire Interface
- Internal Power on Reset
- Low Power Dissipation : 8mW at 5V, 3.6mW at 3V
- Integrated REF Buffer
- Output Range: Twice the Reference Voltage
- Not Sensitive to Temperature
- Software Power down
- Power Supply: 2.7V~5.5V

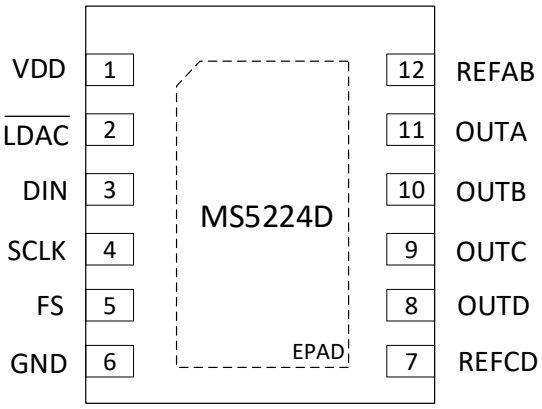
## APPLICATIONS

- Digital Servo System Control
- Digital Compensation and Gain Adjustment
- Industrial Process Control
- Mechanical and Mobile Control Equipment
- High Capacity Storage Device

## PRODUCT SPECIFICATION

| Part Number | Package | Marking |
|---|---|---|
| MS5224D | DFN12 | 5224D |

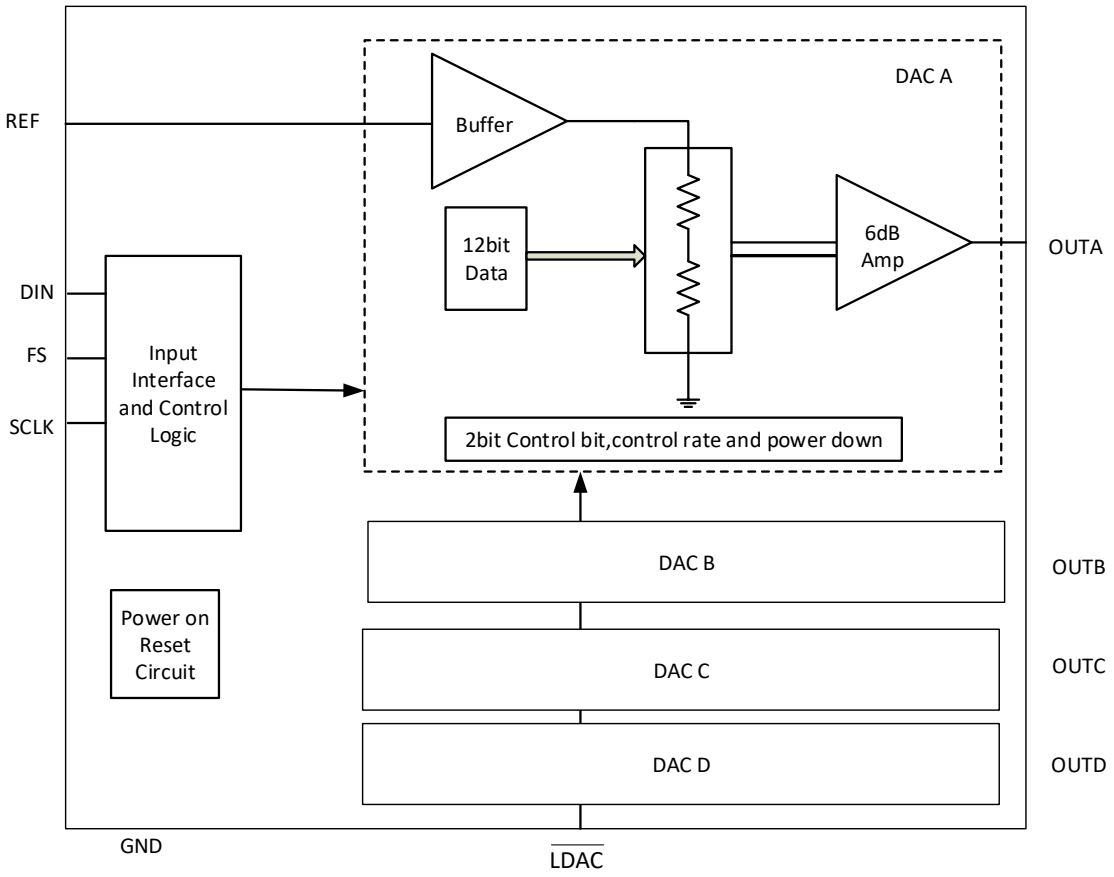
## PIN CONFIGURATION




## PIN DESCRIPTION

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | VDD | - | Power Supply |
| 2 | $\overline{\text{LDAC}}$ | I | When $\overline{\text{LDAC}}$ input is high level, DAC output is not updated.<br>When $\overline{\text{LDAC}}$ input is low level, DAC output is updated.<br>When $\overline{\text{LDAC}}$ is not used, it can remain always low-level. |
| 3 | DIN | I | Serial Data Input |
| 4 | SCLK | I | Serial Digital Clock Input |
| 5 | FS | I | Frame Synchronization Input Signal |
| 6 | GND | - | Ground |
| 7 | REFCD | I | Reference Input Voltage for Channel C and D |
| 8 | OUTD | O | Analog Output for Channel D |
| 9 | OUTC | O | Analog Output for Channel C |
| 10 | OUTB | O | Analog Output for Channel B |
| 11 | OUTA | O | Analog Output for Channel A |
| 12 | REFAB | I | Reference Input Voltage for Channel A and B |
| - | EPAD | - | Thermal Pad, connect to analog ground |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Power Supply | $V_{DD}$ | -0.3 ~ +7 | V |
| Input Digital Voltage | $V_{IN}$ | -0.3 ~ $V_{DD}$+0.3 | V |
| Reference Input Voltage | $V_{REFIN}$ | -0.3 ~ $V_{DD}$+0.3 | V |
| Operating Temperature | $T_A$ | -40 ~ +105 | °C |
| Storage Temperature | $T_{STG}$ | -65 ~ +150 | °C |
| Maximum Junction Temperature | $T_{JMAX}$ | 150 | °C |
| Lead Temperature | $T_{SOLDER}$ | 260 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply | 5V Supply | 4.5 | 5 | 5.5 | V |
| | 3V Supply | 2.7 | 3 | 3.3 | |
| Digital Input High Level ($V_{IH}$) | $V_{DD}$=2.7V | 2 | | | V |
| | $V_{DD}$=5.5V | 2.4 | | | |
| Digital Input Low Level ($V_{IL}$) | $V_{DD}$=2.7V | | | 0.6 | V |
| | $V_{DD}$=5.5V | | | 1 | |
| Reference Voltage | 5V Supply (See Note 1) | 0 | 2.048 | $V_{DD}$-1.5 | V |
| | 3V Supply (See Note 1) | 0 | 1.024 | $V_{DD}$-1.5 | |
| Load Resistance | | 2 | 10 | | kΩ |
| Load Capacitance | | | | 100 | pF |
| SCLK Rate | | | | 20 | MHz |

Note 1: The input voltage greater than $V_{DD}$/2 would result in saturated output at large DAC input codes.

## ELECTRICAL CHARACTERISTICS

**Static DAC**

| Parameter | | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Resolution | | | 12 | | | Bits |
| Integral Non-linearity (INL) | | See Note 1 | | ±1.5 | ±4 | LSB |
| Differential Non-linearity (DNL) | | See Note 2 | | ±0.5 | ±1 | LSB |
| Zero Scale Offset | | See Note 3 | | | ±12 | mV |
| Zero Scale Offset Temperature Drift | | See Note 4 | | 10 | | ppm/°C |
| Gain Error | | See Note 5 | | | ±0.6 | %of FS Voltage |
| Gain Error Temperature Drift | | See Note 6 | | 10 | | ppm/°C |
| PSRR | Zero Scale | See Note 7 and 8 | | -80 | | dB |
| | Full Scale | | | -80 | | dB |

Note:

1. Integrated non-linearity (INL) refers to linearity error, which is the maximum deviation of the output from the ideal output by eliminating zero-scale error and full-scale error.

2. Differential non-linearity (DNL), differential error, refers to the maximum amplitude change adjacent to the LSB.

3. Zero-scale offset refers to the analog output when digital input is zero.

4. Zero-scale temperature drift refers to temperature change of the analog output when digital input is zero.

5. Gain error refers to the deviation between the analog output and ideal output after zero-scale offset is removed.

6. Gain error temperature drift refers to the variation of the deviation between the analog output and ideal output with temperature after zero-scale offset is removed.

7. Zero-scale power supply rejection ratio is the change ratio of output caused by a change in VDD of 5±0.5V and 3±0.3V when the digital input is zero.

8. Full-scale power supply rejection ratio is the change ratio of output caused by a change in VDD of 5±0.5V and 3±0.3V when the digital input is high level.

**DAC Output**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage | $R_L$=10kΩ | 0 | | $V_{DD}$-0.4 | V |
| Output Load Regulation Accuracy | $R_L$=2kΩ to 10kΩ | | 0.1 | 0.25 | %of FS |

**Reference Input Voltage**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage | See Note 9 | 0 | | $V_{DD}$-1.5 | V |
| Input Resistance | | | 10 | | MΩ |
| Input Capacitance | | | | | pF |

| Parameter | Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Reference Feedthrough | $V_{REFIN}$= 1Vpp (1kHz) + 1.024 V (See Note 10) | | | -75 | | dB |
| Reference Input Bandwidth | $V_{REFIN}$ = 0.2Vpp+ 1.024 V (Large Signal) | Slow | | 0.5 | | MHz |
| | | Fast | | 1 | | |

Note:

9. The reference input voltage greater than $V_{DD}$/2 would result in output saturation distortion.

10. Reference feedthrough refers to the analog output rejection ratio when the output is zero and $V_{REFIN}$ = 1Vpp (1kHz) +1.024V.

**Digital Input**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Digital Input High-level Current | $V_I$=$V_{DD}$ | | | ±1 | μA |
| Digital Input Low-level Current | $V_I$=0V | | | ±1 | μA |
| Input Capacitance | | | 3 | | pF |

**Power Dissipation**

| Parameter | Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Supply Current | 5V supply, no load, add CLOCK, all inputs 0V or VDD | Slow | | 1.6 | 2.4 | mA |
| | | Fast | | 3.8 | 5.6 | |
| | 3V supply, no load, add CLOCK, all inputs 0V or VDD | Slow | | 1.2 | 1.6 | mA |
| | | Fast | | 3.2 | 4.8 | |

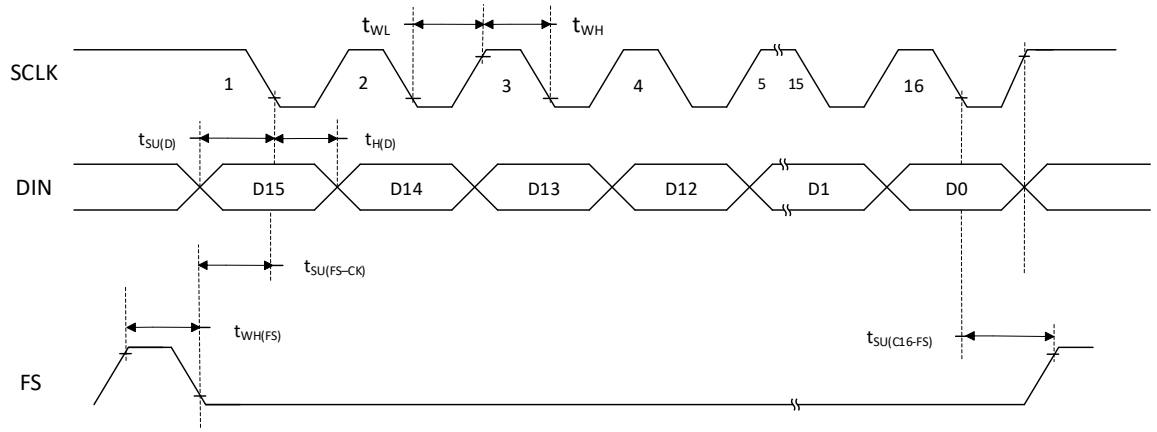
**Analog Output Dynamic**

| Parameter | Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SR | $C_L$=100pF, $R_L$=10kΩ, $V_O$=10% to 90%, $V_{REF}$=2.048,1.024 | Fast | | 5 | | V/μs |
| | | Slow | | 1 | | |
| $t_S$ | To ±0.5LSB, $C_L$=100pF, $R_L$=10kΩ | Fast | | 3 | 5.5 | μs |
| | | Slow | | 9 | 20 | |
| $t_{S(C)}$ | To ±0.5LSB, $C_L$=100pF, $R_L$=1kΩ | Fast | | 1 | | μs |
| | | Slow | | 2 | | |
| Glitch Energy | From 7FF to 800 | | | 10 | | nV-sec |
| SNR | $V_{REF}$=1.024 at 3V; $V_{REF}$=2.048 at 5V, $f_S$=400kSPS, $f_{OUT}$=1.1kHz sine wave, $C_L$=100pF, $R_L$=10kΩ, BW=20kHz | | | 74 | | dB |
| S/(N+D) | | | | 66 | | |
| THD | | | | -68 | | |
| SFDR | | | | 70 | | |

**Digital Input Timing**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Setup Time, FS to the First Falling Edge of SCLK | $t_{SU(FS-CK)}$ | 8 | | | ns |
| Setup Time, the Sixteenth Falling Edge of SCLK after FS low on which bit D0 is sampled before rising edge of FS | $t_{SU(C16-FS)}$ of FS | 10 | | | ns |
| SCLK High Level Duration | $t_{WH}$ | 25 | | | ns |
| SCLK Low Level Duration | $t_{WL}$ | 25 | | | ns |
| Setup Time, Data Ready before Falling Edge of SCLK | $t_{SU(D)}$ | 8 | | | ns |
| Hold Time, Data Held Valid after Falling Edge of SCLK | $t_{H(D)}$ | 5 | | | ns |
| FS High Level Duration | $t_{WH(FS)}$ | 20 | | | ns |

**Timing Diagram**



## APPLICATION DESCRIPTION

The MS5224D is a 12-bit, single-power digital-to-analog converter. Its architecture uses resistance array structure, which integrates serial interface, rate and power down logic control, reference input buffer, resistor string and output rail-to-rail amplifier.

The output voltage can be expressed as:

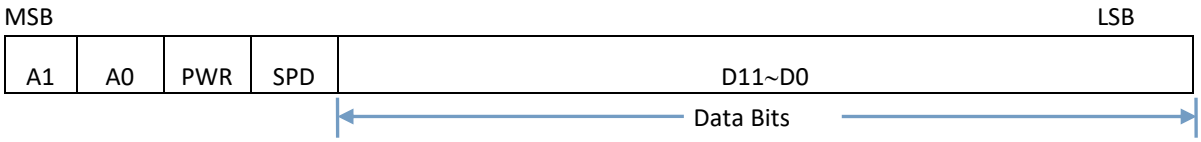
$$V_{OUT}=2\times\frac{V_{REF}\times D}{2^N}$$

**Serial Interface**

The MS5224D starts to input data bit-per-bit on the falling edge of FS (active high at first). After 16 bits have been transferred or when FS becomes high, the internal DAC updates the corresponding output level.

**Data Format**

The data word of the MS5224D consists of two parts: control bits (D15~D12) and data bits(D11~D0).




PWR: Power dissipation control, 1 for off mode, 0 for normal mode.

SPD: Speed control, 1 for fast mode, 0 for slow mode.

A1, A0 are the address selection bits of the internal DAC channels, the truth table is as follows:

| A1 | A0 | DAC Address |
|---|---|---|
| 0 | 0 | DAC-A |
| 0 | 1 | DAC-B |
| 1 | 0 | DAC-C |
| 1 | 1 | DAC-D |

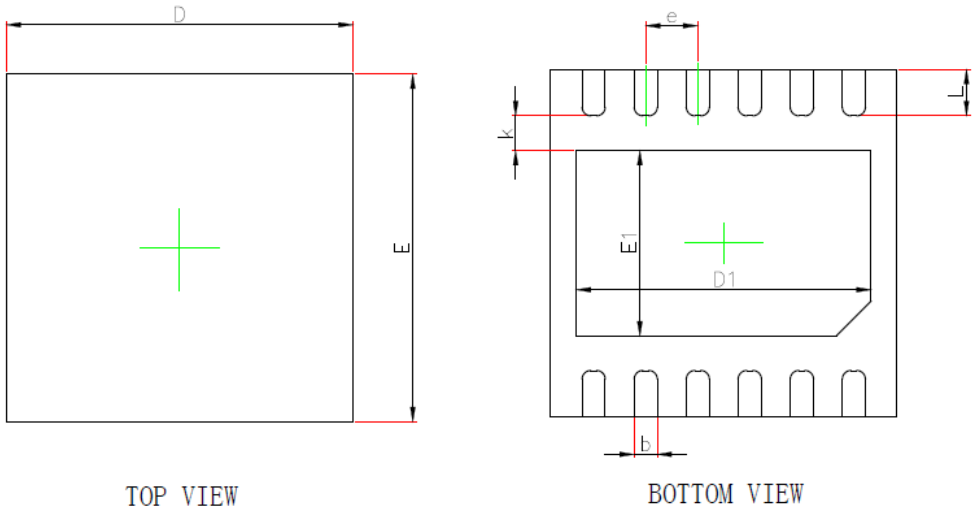
**Power Supply Bypassing and Ground Management**

In order to improve system performance, the analog and digital ground should be connected to different ground planes, which are linked together at low impedance node. It's better to connect DAC AGND to the system analog ground. Thus, the current of analog ground is managed well, and the voltage drop on the analog ground traces could be ignored.

The 0.1μF ceramic decoupling capacitance should be connected between ground and power supply. And it is placed as close to the chip as possible. If magnet ring is used, the analog and digital power supply could be further separated.

## PACKAGE OUTLINE DIMENSIONS

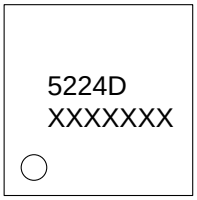
**DFN12**




| Symbol | Dimensions in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.700/0.800 | 0.800/0.900 | 0.028/0.031 | 0.031/0.035 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.203REF | | 0.008REF | |
| D | 2.924 | 3.076 | 0.115 | 0.121 |
| E | 2.924 | 3.076 | 0.115 | 0.121 |
| D1 | 2.450 | 2.650 | 0.096 | 0.104 |
| E1 | 1.500 | 1.700 | 0.059 | 0.067 |
| k | 0.200MIN | | 0.008MIN | |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| e | 0.450TYP | | 0.018TYP | |
| L | 0.324 | 0.476 | 0.013 | 0.019 |

## MARKING and PACKAGING SPECIFICATION

### 1. Marking Drawing Description




Product Name：5224D

Product Code：XXXXXXX

### 2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

### 3. Packaging Specification

| Device | Package | Piece/Reel | Reel/Box | Piece /Box | Box/Carton | Piece/Carton |
|---|---|---|---|---|---|---|
| MS5224D | DFN12 | 5000 | 1 | 5000 | 8 | 40000 |

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**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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