

TMDS Digital Video Equalizer

PRODUCT DESCRIPTION

The MS3815 is an adaptive equalizer integrated chip, which can provide compensations for cable loss of DVI, HDMI, DFP, PanelLink and ADC, extending the distance of transmission cable. The goal of the MS3815 is to equalize TMDS signal.

The MS3815 includes four CML differential input and output channels (three data channels, one clock channel). It also has clock loss indication function. For direct chip to chip communication, output drivers can switch to half of DVI output specification to decrease EMI and power dissipation.

The MS3815 can operate not only in adaptive mode ,but also in manual mode for specific application. The MS3815 adopts 3.3V single power supply and operates in temperature from -20°C to 105°C. The data rate is from 250Mbps to 1.65Gbps.



TQFP48

FEATURES

- Extend Cable Length of Projector or Monitor with DVI, DFP, PanelLink, ADC or HDMI Interface
- Different Wire Diameters of DVI interface in Transmission Cable Length as follows:
24AWG Shielded Twisted Pair: 0-50 meter
28AWG Shielded Twisted Pair: 0-36 meter
30AWG Shielded Twisted Pair: 0-30 meter
- Compatible with Digital TV Resolution for 480i,480p,720p, 1080i,1080p Compatible with VGA,SVGA, XGA,SXGA,UXGA
- Without System Control, Automatically Equalize 40dB Cable Loss at 1650Mbps
- 3.3V Power Supply
- 0.6W Power Dissipation (Typical Value)

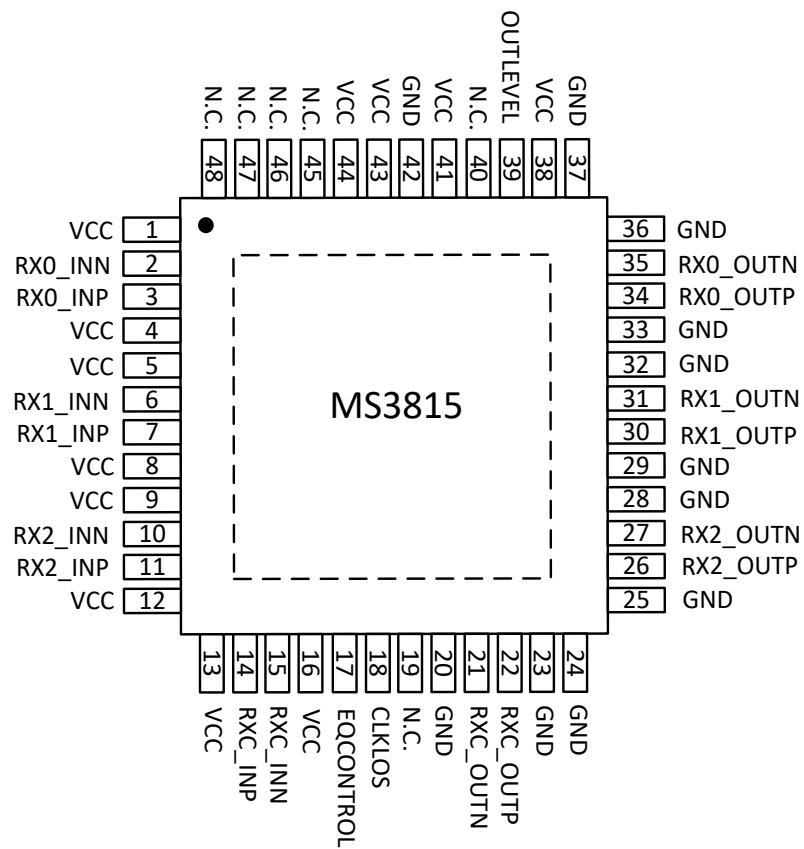
APPLICATIONS

- Projector DVI/HDMI Input Interface
- DVI-D/HDMI Cable Extension Modules and Active Cable Device
- LCD Display

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS3815	TQFP48	MS3815

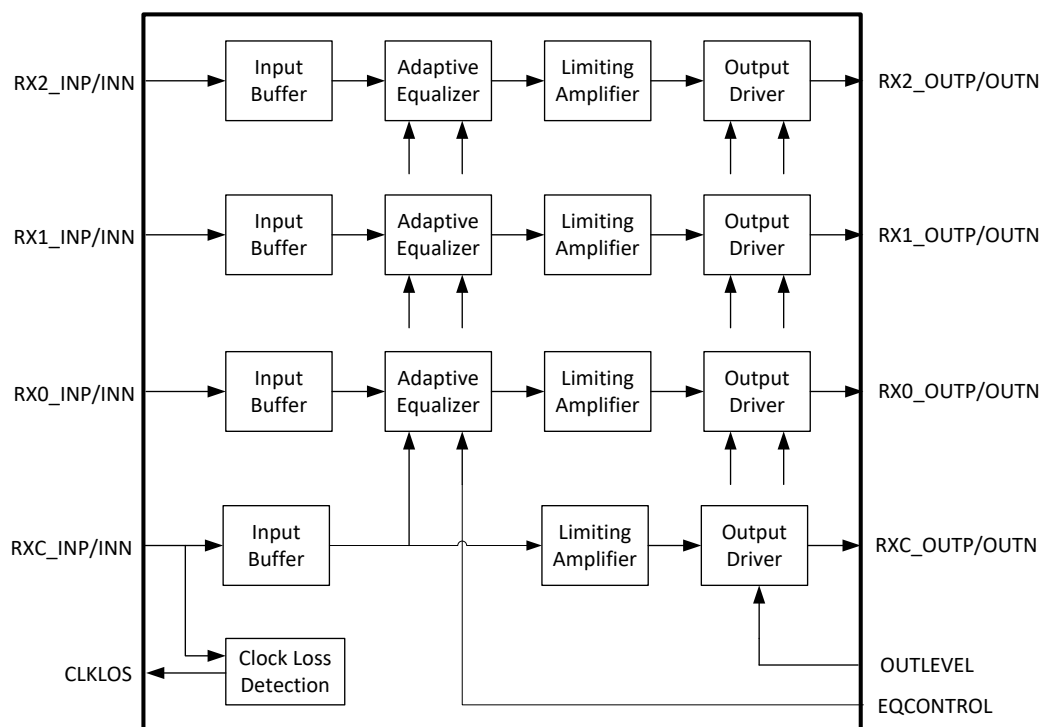
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1,4,5,8,9,12,13, 16,38,41,43,44	VCC	POWER	Power Supply
2	RX0_INN	I	Negative Data Input, CML Level
3	RX0_INP	I	Positive Data Input, CML Level
6	RX1_INN	I	Negative Data Input, CML Level
7	RX1_INP	I	Positive Data Input, CML Level
10	RX2_INN	I	Negative Data Input, CML Level
11	RX2_INP	I	Positive Data Input, CML Level
14	RXC_INP	I	Positive Data Input, CML Level
15	RXC_INN	I	Negative Data Input, CML Level
17	EQCONTROL	I	Equalization Control. The pin allows user to control equalization grade: When pin is grounded: Adaptive Mode; When pin is connected to VCC/2: Minimum Equalization Mode; When pin is connected to the voltage between (VCC-1) to VCC: Manual Mode
18	CLKLOS	O	Clock Signal Loss Detection. LVTTTL LEVEL, Open- Collector Output. The pin indicates that clock input terminal RXC_INP or RXC_INN cable is damaged or good contact.
20,23,24,25,28,29, 32,33,36,37,42	GND	POWER	Ground
21	RXC_OUTN	O	Negative Clock Output, CML Level
22	RXC_OUTP	O	Positive Clock Output, CML Level
26	RX2_OUTP	O	Positive Data Output, CML Level
27	RX2_OUTN	O	Negative Data Output, CML Level
30	RX1_OUTP	O	Positive Data Output, CML Level
31	RX1_OUTN	O	Negative Data Output, CML Level
34	RX0_OUTP	O	Positive Data Output, CML Level
35	RX0_OUTN	O	Negative Data Output, CML Level
39	OUTLEVEL	I	Output Voltage Amplitude Control, LVTTTL LEVEL. When high: Standard DVI Amplitude(1000mV _{PP}) When low: Half of Amplitude
19,40,45,46,47,48	N.C.	-	Not Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Rating	Unit
Power Supply	V _{CC}	-0.5 ~ +4	V
Input and Output Voltage	V _{CCIO}	-0.5 ~ (V _{CC} +0.7)	V
CML Differential Pair Pin Voltage		-3.3V ~ +3.3V	V
Maximum Power Dissipation	P _D	2800	mW
Operating Temperature Range	T _{opr}	-20 ~ +105	°C
Storage Temperature Range	T _{stg}	-55 ~ +150	°C
Lead Temperature Range (10 sec)	T _{TOR}	260	°C

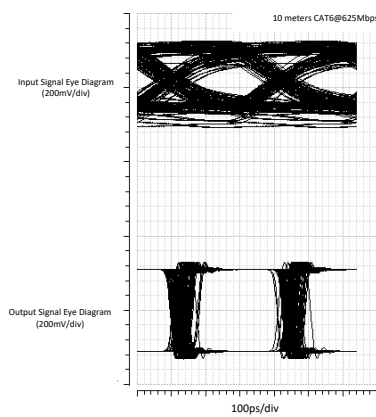
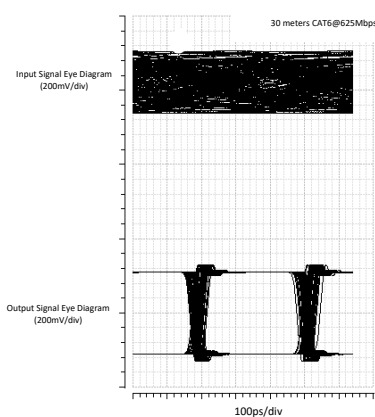
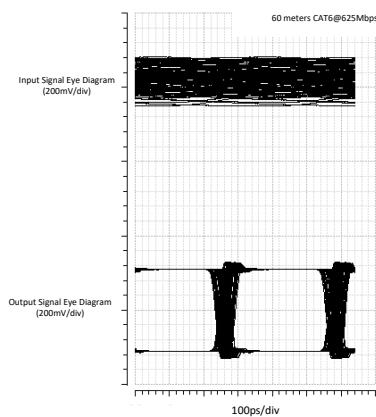
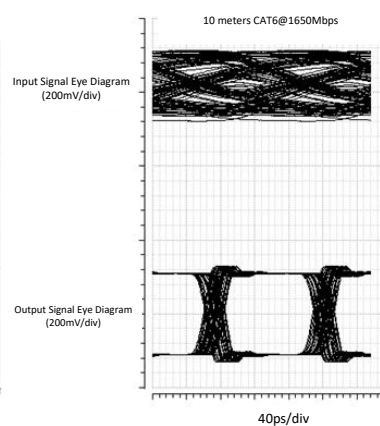
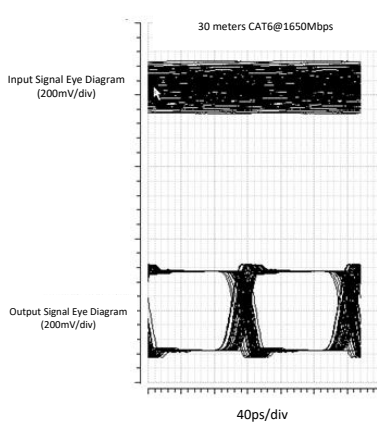
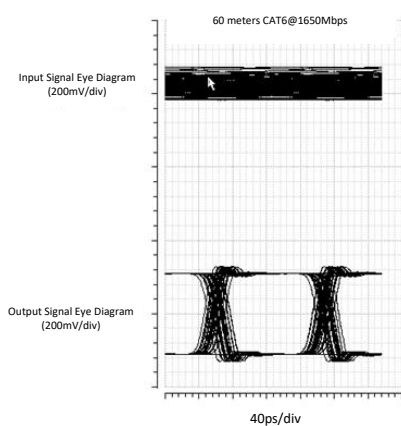
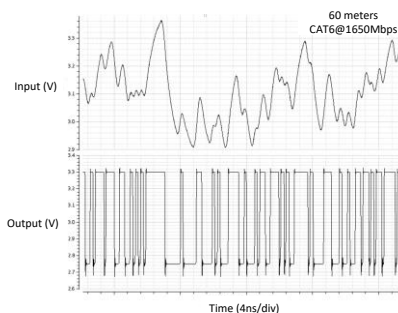
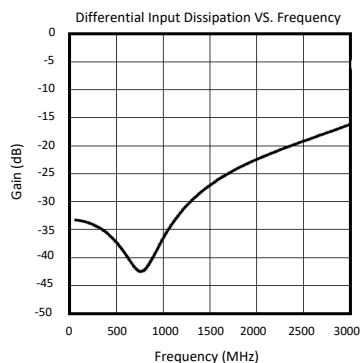
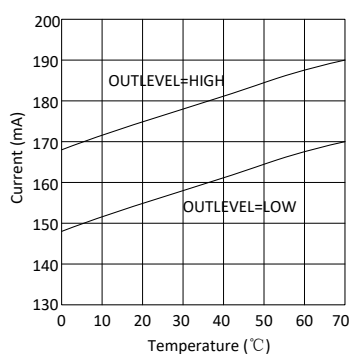
ELECTRICAL CHARACTERISTICS

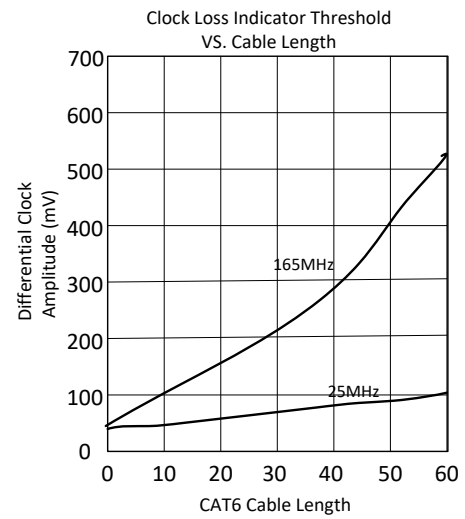
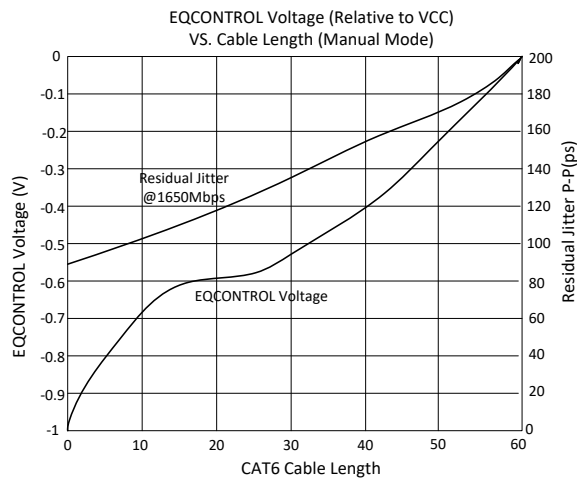
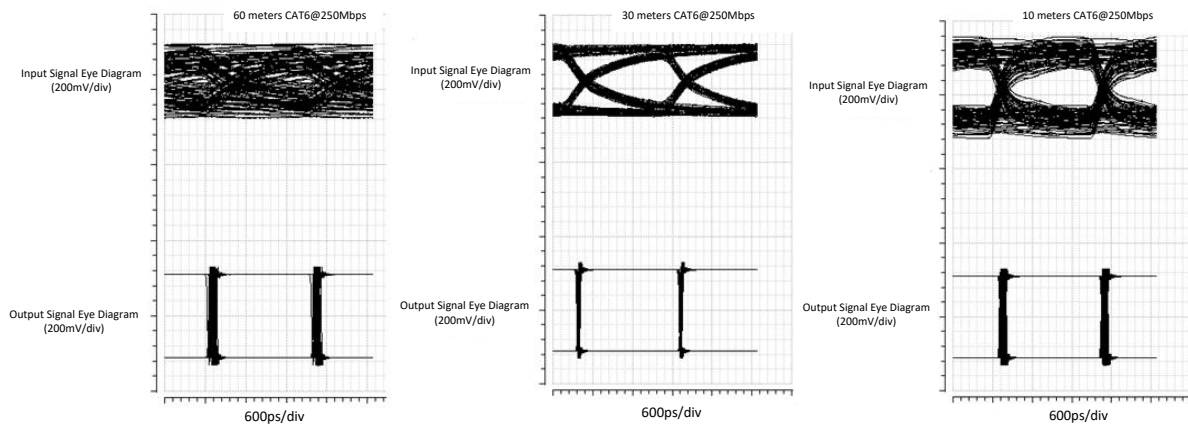
VCC = 3.0V to 3.6V. Typical parameters are VCC=3.3V, external load=50Ω,

TMDs data rate 250Mbps ~ 1650Mbps and T_A=25°C. Unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	VCC		3.0	3.3	3.6	V
Power Supply Current	I _{CC}			198	235	mA
Maximum Power Noise Tolerance		DC~500kHz		200		mV _{P-P}
Data Rate			250		1650	Mbps
Maximum Channel Loss		@825MHz		40		dB
Residual Output Jitter	J _{RD}	250Mbps~1650Mbps			0.25	UI _{P-P}
Tolerate Successive Zero or Single Digit				20		Bits
Control and State						
Differential Voltage Amplitude of Clock Input Terminal when clock indicated pin CLKLOS is bright		165MHz Differential Clock Input		50		mV _{P-P}
CML Input						
Input Different Voltage Amplitude	V _{ID}	Cable Input Terminal	800	1000	1400	mV _{P-P}
Input Common-Mode Voltage	V _{CM}		VCC-0.4		VCC+0.1	V
Input Resistance	R _{IN}	Single Terminal	45	50	55	Ω
CML Output						
Output Different Voltage Amplitude	V _{OD}	50Ω load to VCC OUTLEVEL=HIGH	800	1000	1200	mV _{P-P}
		50Ω load to VCC OUTLEVEL=LOW	350	500	650	mV _{P-P}
Output High Level Voltage	V _{OH}	Single terminal, OUTLEVEL=HIGH		VCC		V
Output Low Level Voltage	V _{OL}	Single terminal, OUTLEVEL=HIGH	VCC-0.6		VCC-0.4	V
Shutdown Voltage	V _{DN}	LEVEL=LOW, PWRDWN=HIGN	VCC-0.01		VCC+0.01	V
Output Common-Mode Voltage	V _{OCM}	Each terminal is connected to VCC with 50Ω load, OUTLEVEL=HIGH		VCC- 0.25		V
Rise/Fall Time	t _{R/F}	20%-80%	70	130	200	ps
LVTTTL Control and Interface						
LVTTTL Input High Level Voltage	V _{IH}		2.0			V
LVTTTL Input Low Level Voltage	V _{IL}				0.8	V
LVTTTL Input High Level Current	I _{IH}	V _{IH} (MIN)<V _{IN} <VCC			-50	μA
LVTTTL Input Low Level Current	I _{IL}	GND<V _{IN} <V _{IL} (MAX)			-100	μA

TYPICAL OPERATION CURVES





FUNCTION DESCRIPTION

The MS3815, TMDS signal equalizer chip accepts CML differential input signal ranging from 250Mbps to 1650Mbps. And it can compensate 40dB loss of coaxial cable at 825MHz, caused by skin effect.

The MS3815 is consist of four CML input buffers, three independent adaptive equalizers, four limiting amplifiers, four output drivers and one clock loss detector.

1. CML Input Buffer and Output Driver

Input buffer and output drivers are all use current mode logic (CML).Output drivers are open-collector. And it can use OUTLEVEL pin to halve output amplitude, in order to be compatible with different interfaces.

2. Clock Loss Detector

When clock input terminal isn't connected well, clock loss detector circuit would drive external LED.

3. Adaptive Equalizer

Each of three data channels has an independent adaptive equalizer. Every channel could determine equalization according to input signal.

4. Limiting Amplifier

Limiting amplifier would amplify output signal from adaptive equalizer, then limit the output amplitude, and finally send to output driver.

5. Application Information

Typical shielded or unshielded twisted pair shows skin effect loss, which could cause high-frequency component loss of TMDS signal, finally lead to error code in long-distance transmission and even result in full close of output signal eye diagram. According to different compensations for different frequency components, the MS3815 recover input signal to open eye diagram.

Basic TMDS signal is consist of four different signal channels ,in which three channels transmit data up to 1650Mbps, and the fourth channel transmits clock signal.The data rate is a tenth of clock, whose maximum frequency is 165MHz.As analogue nVGA link, TMDS must process video signals of different resolutions and date rate. The actual digital signal rate is about from 250Mbps to 1650Mbps. As for super-high resolution application (such as QXGA), which needs two MS3815s, made of six data channels and one clock channel shown as figure 1.

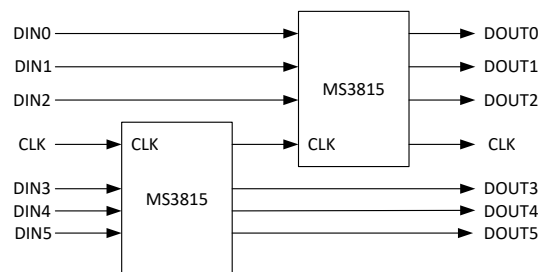


Figure 1. Double Chips Application Scheme

6. Clock Loss Detector

The clock loss detection outputs from CLKLOS pin. When CLKLOS pin outputs low level, it represents signal amplitude of clock input terminal (RXC_INN, RXC_INP) is less than threshold value. When the amplitude is

more than the threshold, CLKLOS pin would output high level. The CLKLOS indicator light would be bright, when the following situations happen, such as broken cable, defective front-stage output drive, or bad-connection clock input terminal. As shown in figure2, CLKLOS makes LED open or close according to driving external inverter.

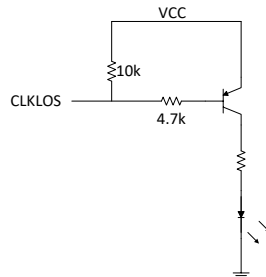


Figure 2. CLKLOS Terminal Output Connection

7. Output Level Control

OUTLEVEL is LVTTTL input pin, which makes user to select standard CML differential amplitude (1000mVPP) or half of that. When the pin is connected to high level, corresponding to standard amplitude. When the pin is connected to low level, corresponding to half of amplitude.

8. Equalization Input Control

EQCONTROL pin allows user to apply the MS3815 according to the next three methods: When the pin is connected to ground, the MS3815 is in adaptive mode; When the pin is connected to the half of VCC, the MS3815 is in minimum equalization mode; When the pin is connected to the level between (VCC-1) and VCC, the MS3815 is in manual mode.

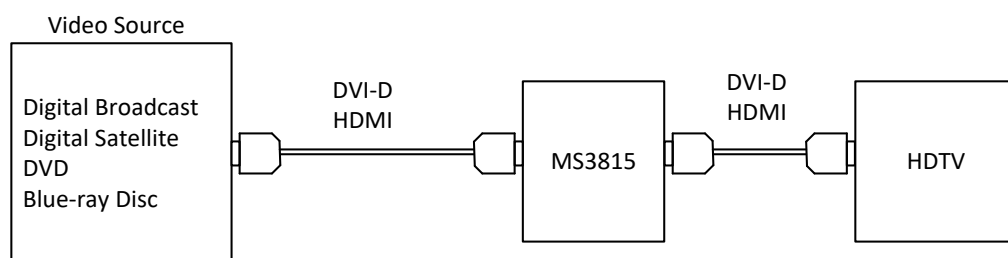
9. Cable Option

The performance of the MS3815 depends on the cable quality. The exchange from difference to common-mode would cause deterministic jitter, which results from two twined wires or unbalanced dielectric.

10. Trace Consideration

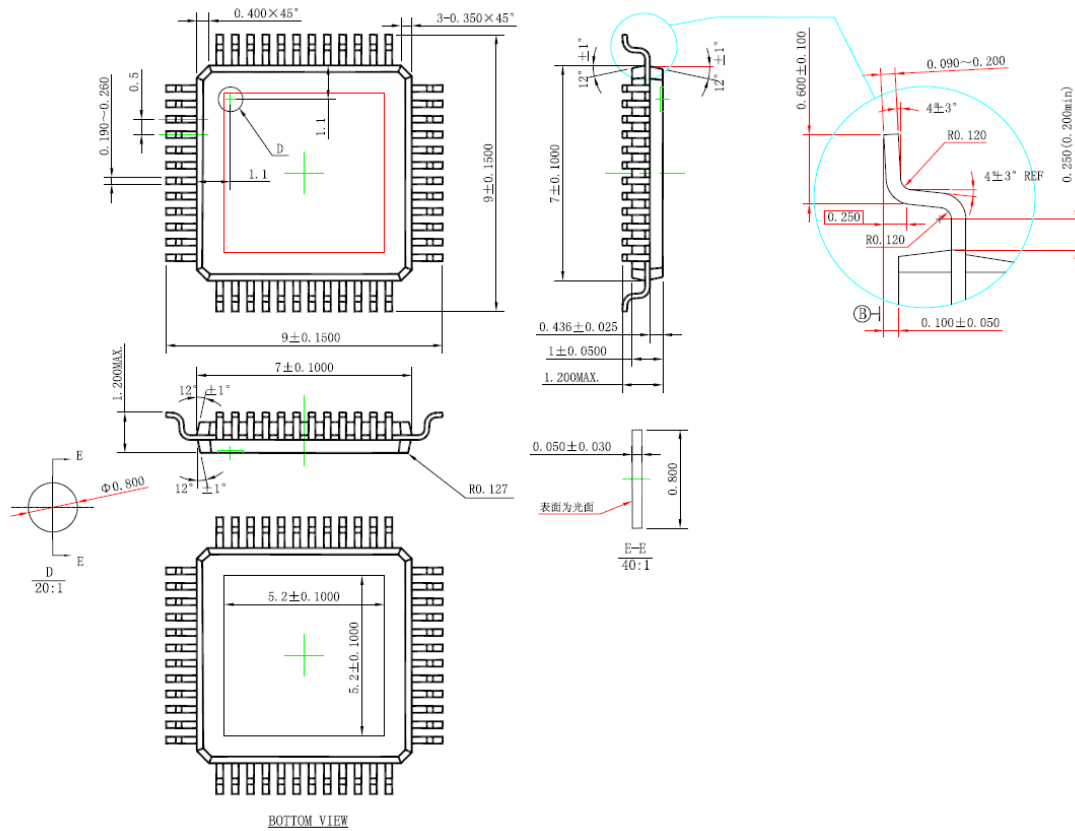
- It should route directly between cable and the MS3815's data and clock input pin, avoiding joint or discontinuous spot.
- Each pair of input and output should be differential, and didn't change phase difference of differential pair by routing as far as possible.
- There are four times more distance among differential pair than the height of dielectric.
- The design of input and output data channel is just for reference, and polar distribution can exchange.
- Continuous ground plane should be placed under high-speed I/O.
- The contact of ground wire should be close to input and output interface, in order to generate the current loop from the MS3815 to cable.
- Maintain 100 Ω differential resistance in data input and output terminal of the MS3815.
- Recommend 200 Ω back resistance to be close to corresponding output terminal of the MS3815, so as to minimize reflection.
- Apply multi-layer PCB to decrease EMI and crosstalk, which has outstanding high-frequency trace technology and no-interference ground wire route.
- Bypass capacitor should be as close to power plane as possible to decrease parasitism.

TYPICAL APPLICATION DIAGRAM



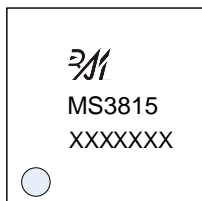
PACKAGE OUTLINE DIMENSIONS

TQFP48



MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: MS3815

Product Code: XXXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Tray	Tray/Box	Piece /Box	Box/Carton	Piece/Carton
MS3815	TQFP48	250	10	2500	4	10000

STATEMENT

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**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



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