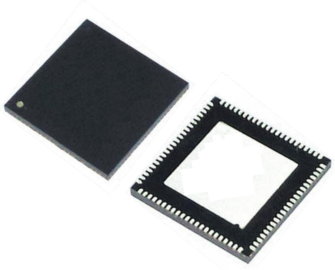
Low Power Dissipation Glucometer SOC

PRODUCT DESCRIPTION

The MS616F187 is a glucometer test SOC, which integrates high performance ADC, high precision operational amplifier, low impedance switch, high precision reference voltage generating circuit and glucose test AC signal circuit. It also integrates I^2C communication protocol. These features make peripherals much less and users just need to operate and read data via interface, thus completing glucose acquisition.

The operating voltage ranges from 2.5V to 3.6V. The temperature range is from -40°C to +85°C. And the MS616F187 is available in a QFN88 package.



QFN88

FEATURES

- Maximum 16bit No Missing Codes Resolution
- ADC INL : 0.01%
- Integrated Oscillator
- Continuous Conversion and Single Conversion
- Integrated Low Offset Operational Amplifier
- Optional Internal and External References
- I^2C Interface
- Low Power Dissipation : 1400uA
- QFN88 Package (Back Thermal Pad)

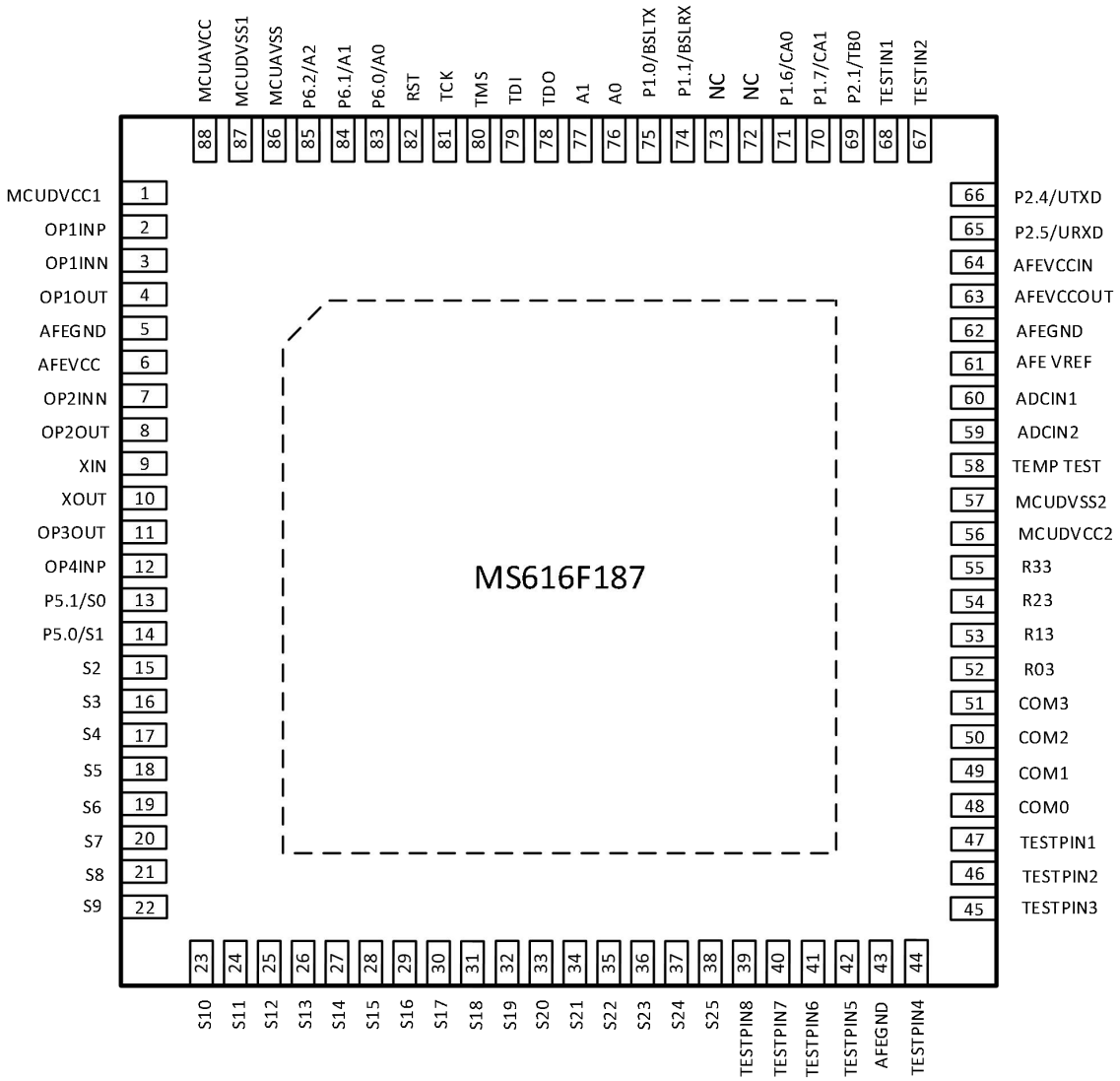
APPLICATIONS

- Glucose Measurement
- Industry Measurement

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS616F187	QFN88	MS616F187

PIN CONFIGURATION



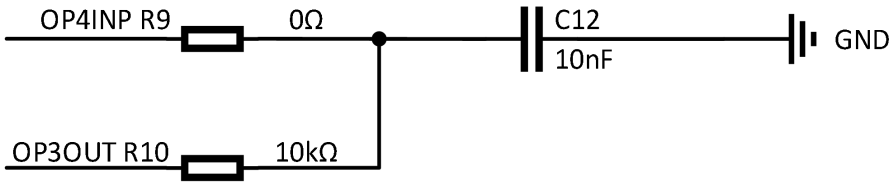
IN DESCRIPTION

Pin	Name	Type	Description
1	MCU DVCC1	-	MCU Digital Power Supply 1
2	OP1INP	I	Positive Input for Amplifier 1
3	OP1INN	I	Negative Input for Amplifier 1
4	OP1OUT	I/O	Output for Amplifier 1
5	AFE GND	-	Ground
6	AFE VCC	-	Power Supply Decoupling Pin, External Capacitance
7	OP2INN	I	Negative Input for Amplifier 2
8	OP2OUT	I/O	Output for Amplifier 2
9	XIN	I	Input Terminal for Crystal Oscillator XT1, can connect with standard crystal and clock crystal
10	XOUT	O	Output Terminal for Crystal Oscillator XT1
11	OP3OUT	O	Output for Amplifier 3, external detection resistor and capacitor network (See Note)
12	OP4INP	I	Buffer Input for Peak Detection (See Note)
13	P5.1/S0	I/O	General Digital I/O Interface / LCD Segment Output 0
14	P5.0/S1	I/O	General Digital I/O Interface / LCD Segment Output 1
15	S2	O	LCD Segment Output 2
16	S3	O	LCD Segment Output 3
17	S4	O	LCD Segment Output 4
18	S5	O	LCD Segment Output 5
19	S6	O	LCD Segment Output 6
20	S7	O	LCD Segment Output 7
21	S8	O	LCD Segment Output 8
22	S9	O	LCD Segment Output 9
23	S10	O	LCD Segment Output 10
24	S11	O	LCD Segment Output 11
25	S12	O	LCD Segment Output 12
26	S13	O	LCD Segment Output 13
27	S14	O	LCD Segment Output 14
28	S15	O	LCD Segment Output 15
29	S16	O	LCD Segment Output 16
30	S17	O	LCD Segment Output 17
31	S18	O	LCD Segment Output 18

Pin	Name	Type	Description
32	S19	O	LCD Segment Output 19
33	S20	O	LCD Segment Output 20
34	S21	O	LCD Segment Output 21
35	S22	O	LCD Segment Output 22
36	S23	O	LCD Segment Output 23
37	S24	O	LCD Segment Output 24
38	S25	O	LCD Segment Output 25
39	TESTPIN8	I	Test Terminal 8. By register setting and peripherals, the resistance value between TESTPIN8 and TESTPIN7 can be measured
40	TESTPIN7	I/O	AC Small Signal Output and Resistor Test Terminal. By register setting and peripherals, the resistance values between TESTPIN7 and TESTPIN2, TESTPIN4, TESTPIN6, TESTPIN8.
41	TESTPIN6	I	Test Terminal 6. By register setting and peripherals, the resistance value between TESTPIN6 and TESTPIN7 can be measured
42	TESTPIN5	I	By register setting and peripherals, test DC current
43	AFE GND	-	Ground
44	TESTPIN4	I	Test Terminal 4. By register setting and peripherals, the resistance value between TESTPIN4 and TESTPIN7 can be measured
45	TESTPIN3	I	Test Terminal 3. By register setting and peripherals, the resistance value between TESTPIN2 and TESTPIN3 can be measured
46	TESTPIN2	I	Test Terminal 2. By register setting and peripherals, the resistance value between TESTPIN2 and TESTPIN3 can be measured
47	TESTPIN1	I	By register setting and peripherals, test peak value of AC signal
48	COM0	O	COM0−3 Used for LCD Common Output
49	COM1	O	COM0−3 Used for LCD Common Output
50	COM2	O	COM0−3 Used for LCD Common Output
51	COM3	O	COM0−3 Used for LCD Common Output
52	R03	I	Analog LCD Level, the Fourth (Minimum) High Input Voltage (V5)
53	R13	I	Analog LCD Level, the Third High Input Voltage (V4 or V3)
54	R23	I	Analog LCD Level, the Second High Input Voltage (V2)
55	R33	I	Analog LCD Level, the Maximum High Input Voltage (V1)
56	MCU DVCC2		MCU Digital Power Supply 2
57	MCU DVSS2		MCU Digital Ground 2
58	TEMP TEST	I	Temperature Test Input, external shunt resistor and thermistor
59	ADCIN2	I	ADC Input 2

Pin	Name	Type	Description
60	ADCIN1	I	ADC Input 1
61	AFE VREF	I/O	2.048V Reference Input or Output
62	AFE GND	-	Ground
63	AFE VCCOUT	I/O	AFE Internal Voltage Decoupling Terminal, external 10uF capacitor
64	AFE VCCIN	-	AFE Power Supply
65	P2.5/URXD	I/O	General Digital I/O Interface / In UART Mode, USART0 Receiving Data Input
66	P2.4/UTXD	I/O	In UART Mode, USART0 Transmitting Data Output
67	TESTIN2	I	Internal Test Terminal 2
68	TESTIN1	I	Internal Test Terminal 1
69	P2.1/TB0	I/O	General Digital I/O Interface / Capture Input of Timer_B7 CCR0 : CCI0A/CCI0B, Compare Output: Out0
70	P1.7/CA1	I/O	General Digital I/O Interface / Comparator A Input
71	P1.6/CA0	I/O	General Digital I/O Interface / Comparator A Input
72	NC	--	Not Connection
73	NC	--	Not Connection
74	P1.1/BSLRX	I/O	General Digital I/O Interface / BSL Input
75	P1.0/BSLTX	I/O	General Digital I/O Interface / BSL Output
76	A0	I	Internal ADC Address 0
77	A1	I	Internal ADC Address 1
78	TDO	O	Test Data Output
79	TDI/TCLK	I	Test Data Input / Test Clock Input
80	TMS	I	Test Mode Selection. TMS is used as input terminal for programming and testing
81	TCK	I	Test Clock. TCK is clock input terminal for programming and testing
82	RST	I	Reset Input
83	P6.0/A0	I/O	General Digital I/O Interface / 12-bit ADC Analog Input A0
84	P6.1/A1	I/O	General Digital I/O Interface / 12-bit ADC Analog Input A1
85	P6.2/A2	I/O	General Digital I/O Interface / 12-bit ADC Analog Input A2
86	MCU AVSS	-	MCU Analog Power Supply
87	MCU DVSS1	-	MCU Digital Ground 1
88	MCU AVCC	-	MCU Analog Ground

Note : PIN11 and PIN12 connection are shown as follows:



Internal Connection

MCU Pin	AFE Pin	Description
P1.2/TA1	SCL	I^2C Control, MCU to AFE
P1.3/TBOUT/SVSOUT	SDA	
P1.4/TBCLK/SMCLK	DRDY	Complete one conversion, pulse signal into MCU
P1.5/TACLK/ACLK	TOMCU	AFE detects test paper inserted, then outputs low level to MCU
P2.0/TA2	REFSEL	AFE Reference Voltage Select Terminal. Low-level selects external reference; high-level selects internal reference
P2.2/TB1	CLK3.2K	MCU outputs 3.2kHz Square Wave Signal to AFE
P2.3/TB2	PCON2	MCU controls internal power switch of AFE, active low

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Range	Unit
Voltage Difference, Vcc to Vss	-0.3 ~ +4.1	V
Input Voltage	-0.3 ~ VCC+0.3	V
Device Diode Current	±2	mA
Operating Temperature (No Programming)	-55 ~ 150	°C
Storage Temperature (Programming)	-40 ~ 85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
MCU Power Supply	AVCC DVCC	Program executing	1.8		3.6	V
		Program executing and SVS enabled, PORON=1	2.0		3.6	V
		Flash Programming	2.7		3.6	V
MCU Power Supply	VSS		0		0	V
TDC Power Supply	VCC		2.5		3.6	V
Operating Temperature	T_A		-40		85	°C
LFXT1 Crystal Frequency	f_{LFXT1}	XTS_FLL=0, Quartz Oscillator		32.768		kHz
		XTS_FLL=1, Ceramic Oscillator	450		8000	kHz
		XTS_FLL=1, Crystal Oscillator	1000		8000	kHz
XT2 Crystal Frequency	f_{XT2}	Ceramic Oscillator	450		8000	kHz
		Crystal Oscillator	1000		8000	kHz
System Clock Frequency	f_{System}	Vcc=3.6V	DC		4	MHz

1. It's recommended to use the same power supply for AVCC and DVCC. The voltage difference between AVCC and DVCC can't exceed 0.3V.
2. When the power supply enough lows to trigger POR, the corresponding voltage is the minimum operating voltage. When the power supply increases to the value, which is equal to the minimum voltage value plus SVS hysteresis voltage, POR signal stops.
3. In LF mode, the LFXT1 oscillator needs to connect with one quartz oscillator externally . When in XT1 mode, LFXT1 needs to connect with one external ceramic or crystal oscillator.

ELECTRICAL CHARACTERISTICS

MCU Supply Current into AVCC + DVCC Except External Current

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Operation Mode (Note 1) $f_{MCLK}=f_{SMCLK}$=1MHz, f_{ACLK}=32768Hz XTS_FLL=0, SELM=(0,1)	I_{AM}	T_A=-40°C to 85°C	VCC=2.2V		280	350	µA
			VCC=3V		420	560	
Low Power Dissipation Mode (Note 1,4)	I_{LPM0}	T_A=-40°C to 85°C	Vcc=2.2V		32	45	µA
			Vcc=3V		55	70	
Low Power Dissipation Mode (Note 2,4) $f_{MCLK}=f_{SMCLK}$=0MHz f_{ACLK}=32768Hz, SCG=0	I_{LPM2}	T_A=-40°C to 85°C	Vcc=2.2V		11	14	µA
			Vcc=3V		17	22	
Low Power Dissipation Mode (Note 3,4) $f_{MCLK}=f_{SMCLK}$=0MHz f_{ACLK}=32768Hz, SCG=1	I_{LPM3}	T_A=-40°C	Vcc=2.2V		1	1.5	µA
		T_A=25°C			1.1	1.5	
		T_A=60°C			2	3	
		T_A=85°C			3.5	6	
		T_A=-40°C	Vcc=3V		1.8	2.2	µA
		T_A=25°C			1.6	1.9	
		T_A=60°C			2.5	3.5	
		T_A=85°C			4.2	7.5	
Low Power Dissipation Mode (Note 2,4) $f_{MCLK}=f_{SMCLK}$=0MHz f_{ACLK}=0Hz, SCG=1	I_{LPM4}	T_A=-40°C	Vcc=2.2V		0.1	0.5	µA
		T_A=25°C			0.1	0.5	
		T_A=60°C			0.7	1.1	
		T_A=85°C			1.7	3	
		T_A=-40°C	Vcc=3V		0.1	0.5	µA
		T_A=25°C			0.1	0.5	
		T_A=60°C			0.8	1.2	
		T_A=85°C			1.9	3.5	

Note:

1. Timer_B frequency is locked as $f_{DCOCLK}=f_{DCO}$=1MHz. All inputs are connected to 0V or Vcc. All outputs have no source or reverse current.

2. All inputs are connected to 0V or Vcc. All outputs have no source or reverse current.

3. All inputs are connected to 0V or Vcc. All outputs have no source or reverse current. The current consumption of LPM3 is achieved by measuring the operating current of timer 1 and LCD (select ACLK). Comparator A and the current in SVS module would be described specially.

4. Including the current consumption in BROWNOUT module.

In operation mode, the relationship between consumption current and system frequency:

$$I_{AM} = I_{AM\ [1\ MHz]} \times f_{System\ [MHz]}$$

In operation mode, the relationship between consumption current and power supply:

$$I_{AM} = I_{AM\ [3\ V]} + 175\ \mu A/V \times (V_{CC} - 3\ V)$$

MCU Schmitt Trigger Input Terminal——P1, P2, P5, P6

Parameter	Symbol	Power Supply	Min	Typ	Max	Unit
Forward Input Threshold Voltage	V_{IT+}	2.2 V	1.1		1.5	V
		3 V	1.5		1.9	
Reverse Input Threshold Voltage	V_{IT-}	2.2 V	0.4		0.9	V
		3 V	0.9		1.3	
Input Hysteresis ($V_{IT+} - V_{IT-}$)	V_{hys}	2.2 V	0.3		1.1	V
		3 V	0.5		1	

MCU Standard Input Terminal——RST/NMI, JTAG (TCK, TMS, TDI, TDO)

Parameter	Symbol	Power Supply	Min	Typ	Max	Unit
Low Level Input Voltage	V_{IT+}	2.2V/3V	VSS		VSS+0.6	V
High Level Input Voltage	V_{IT-}		0.8VCC		VCC	V

MCU Input Terminal——Px.x, TAx, TBx

Parameter	Symbol	Power Supply	Power Supply	Min	Typ	Max	Unit
External Interrupt Timing	$t_{(int)}$	Terminal P1, P2: P1.x to P2.x, External triggering signal is interrupt flag (Note 1)	2.2V/3V	1.5			cycle
			2.2V	62			ns
			3V	50			
Timer_A, Timer_B Capture Time	$t_{(cap)}$	TA0,TA1,TA2 TB0,TB1,TB2,TB3,TB4,TB5,TB6	2.2V	62			ns
			3V	62			
Clock Frequency applied to Timer_A/B	$f_{(TAext)}$	TACLK, TBCLK, INCLK: $t_{(H)} = t_{(L)}$	2.2V			8	MHz
	$f_{(TBext)}$		3V			10	
Clock Frequency of Timer_A/B	$f_{(TAint)}$	Select SMCLK or ACLK	2.2V			8	MHz
	$f_{(TBint)}$		3V			10	

Note 1: When external signal sets interrupt flag, the corresponding t(int) is even with trigger signal shorter than t(int). The clock cycle and time parameter must be simultaneously met to ensure interrupt flag setting. t(int) is measured referred to MCLK cycle.

MCU Leakage Current (Note 1,2)

Parameter	Symbol	Condition	Power Supply	Min	Max	Unit
Leakage Current	I_{lkg}	Px Terminal： $V_{(Px.x)}$	2.2/3V		50	nA

Note :

1. Leakage current is measured when VSS or VCC is applied to relative pins, unless otherwise noted.
2. The terminal pin must be set as input , and couldn't have any pull-up or pull-down resistor.

MCU Output Terminal——P1, P2, P5, P6

Parameter	Symbol	Condition	Power Supply	Min	Typ	Max	Unit
High Level Output Voltage	V_{OH}	$I_{OH(max)}$ =−1.5mA (Note 1)	2.2V	VCC0.25		VCC	V
		$I_{OH(max)}$ =−6mA (Note 2)	2.2V	VCC-0.6		VCC	
		$I_{OH(max)}$ =−1.5mA (Note 1)	3V	VCC0.25		VCC	
		$I_{OH(max)}$ =−6mA (Note 2)	3V	VCC-0.6		VCC	
Low Level Output Voltage	V_{OL}	$I_{OL(max)}$ =1.5mA (Note 1)	2.2V	VSS		VSS+0.25	V
		$I_{OL(max)}$ =6mA (Note 2)	2.2V	VSS		VSS+0.6	
		$I_{OL(max)}$ =1.5mA (Note 1)	3V	VSS		VSS+0.25	
		$I_{OL(max)}$ =6mA (Note 2)	3V	VSS		VSS+0.6	

Note :

1. $I_{OH(max)}$and $I_{OL(max)}$ are the maximum total current, the sum of all output currents. Only when it is less than 12mA, just meet maximum voltage without drop.
2. $I_{OH(max)}$and $I_{OL(max)}$are the maximum total current, the sum of all output currents. Only when it is less than 48mA, just meet maximum voltage without drop.

MCU Output Frequency

Parameter		Condition		Min	Typ	Max	Unit
$f_{(Px.y)(1≤x≤6,0≤y≤7)}$		C_L=20pF, I_L=1.5mA	V_{CC} = 2.2 V	DC		5	MHz
			V_{CC} = 3 V	DC		7.5	
$f_{(ACLK)}$		C_L = 20 pF				$f_{(System)}$	MHz
$f_{(MCLK)}$							
$f_{(SMCLK)}$							
$t_{(Xdc)}$	Output Duty Cycle	P1.5/TACLK/CLK, C_L=20pF, VCC=2.2V/3V	$f_{(ACLK)}=f_{(LFXT1)}=f_{(XT1)}$	40%		60%	
			$f_{(ACLK)}=f_{(LFXT1)}=f_{(LF)}$	30%		70%	
			$f_{(ACLK)}=f_{(LFXT1)}$		50%		
		P1.1/TA0/MCLK, C_L=20pF, VCC=2.2V/3V	$f_{(MCLK)}= f_{(XT1)}$	40%		60%	
			$f_{(MCLK)}=f_{(DCOCLK)}$	50%-15ns	50%	50%+15ns	
		P1.4/TBCLK/SMCLK, C_L=20pF, VCC=2.2V/3V	$f_{(SMCLK)}=f_{(XT2)}$	40%		60%	
			$f_{(SMCLK)}= f_{(DCOCLK)}$	50%-15ns	50%	50%+15ns	

MCU Wake-up Mode LPM3

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Delay Time	$t_{d(LPM3)}$	f = 1 MHz	2.2V/3V			6	μs
		f = 2 MHz				6	
		f = 3 MHz				6	

RAM

Parameter	Condition	Min	Typ	Max	Unit
VRAMh	CPU Stop State (Note 1)	1.6			V

Note 1: The parameter defines the minimum power supply when RAM changes. And all programme must stop when measuring the parameter.

LCD

Parameter		Condition		Min	Typ	Max	Unit
Analog Voltage	$V_{(33)}$	P5.7/R33 Voltage	VCC=3V	2.5		VCC+0.2	V
	$V_{(23)}$	P5.6/R23 Voltage			$[V_{(33)}-V_{(03)}] \times 2/3 + V_{(03)}$		V
	$V_{(13)}$	P5.5/R13 Voltage			$[V_{(33)}-V_{(03)}] \times 2/3 + V_{(03)}$		V
	$V_{(33)}$-$V_{(03)}$	R33 to R03 Voltage		2.2		VCC+0.2	V
Input Leakage Current	$I_{(R03)}$	R03=VSS	No loads on all control and common terminals, VCC=3V			20	nA
	$I_{(R13)}$	P5.5/R13=VCC/3				20	nA
	$I_{(R23)}$	P5.6/R23=2VCC/3				20	nA
Segment Address Voltage	$V_{(Sxx0)}$	I(Sxx) = -3μA，VCC=3V		$V_{(03)}$		$V_{(03)}$-0.1	V
	$V_{(Sxx1)}$			$V_{(13)}$		$V_{(13)}$-0.1	V
	$V_{(Sxx2)}$			$V_{(23)}$		$V_{(23)}$-0.1	V
	$V_{(Sxx3)}$			$V_{(33)}$		$V_{(33)}$-0.1	V

MCU Comparator A (Note 1)

Parameter	Condition	Power Supply	Min	Typ	Max	Unit
$I_{(CC)}$	CAON=1,CARSEL=0,CAREF=0	2.2V		25	40	μA
		3V		45	60	
$I_{(Refladder/RefDiode)}$	CAON=1, CARSEL=0, CAREF=1/2/3, No load at P1.6/CA0 and P1.7/CA1	2.2V		30	50	μA
		3V		45	71	
$V_{(Ref025)}$	PCA0=1, CARSEL=1, CAREF=1, No load at P1.6/CA0 and P1.7/CA1	2.2 V / 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	PCA0=1, CARSEL=1, CAREF=2, No load at P1.6/CA0 and P1.7/CA1	2.2V / 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	PCA0=1, CARSEL=1, CAREF=3, No load at P1.6/CA0 and P1.7/CA1; T_A = 85°C	2.2 V	390	480	540	mV
		3 V	400	490	550	
Common-mode Input Voltage (V_{IC})	CAON=1	2.2 V / 3 V	0		VCC-1	V
Offset Voltage (V_p–V_S)	Note 2	2.2 V / 3 V	-30		30	mV
V_{hys}	CAON = 1	2.2 V / 3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$	T_A = 25 °C, Overdrive 10 mV, without filter: CAF = 0	2.2 V	160	210	300	ns
		3 V	80	150	240	
	T_A = 25 °C, Overdrive 10 mV, with filter: CAF = 1	2.2 V	1.4	1.9	3.4	μs
		3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$	T_A = 25 °C, Overdrive 10 mV, without filter: CAF = 0	2.2 V	130	210	300	ns
		3 V	80	150	240	
	T_A = 25 °C, Overdrive 10 mV, with filter: CAF = 1	2.2 V	1.4	1.9	3.4	μs
		3 V	0.9	1.5	2.6	

Note:

1. The leakage current of comparator A has been defined in Ilkg(Px.x).

2. By setting CAEX bit, make the comparator A input reverse. And measure twice continuously, the input offset voltage could be cancelled, then add the two measurements.

POR/Brownout Reset(BOR) (Note 1)

Parameter		Condition	Min	Typ	Max	Unit
$t_{d(BOR)}$	Brownout (Note 2)				2000	us
$V_{CC(start)}$		$dV_{CC}/dt \le 3$ V/s		$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s			1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s	70	130	180	mV
$t_{(reset)}$		Pulse width needed at RST/NMI pin to reset internally, V_{CC} = 2.2 V/3 V	2			us

Note:

1. The current consumed in Brownout module has been included in total currents Icc. The voltage range is : $V_{(B\_IT-)} + V_{hys(B\_IT-)} \leq 1.8V$.

2. After $V_{CC}=V_{(B\_IT-)}+V_{hys(B\_IT-)}$, CPU starts to execute program after one $t_{d(BOR)}$ cycle. Before $V_{CC} \geq V_{CC(min)}$, FLL+ setting can't change. $V_{CC(min)}$ is the minimum power supply at operating frequency.

MCU Supply Voltage Supervision

Parameter	Condition		Min	Typ	Max	Unit
$t_{(SVSR)}$	$dV_{CC}/dt \geq 30$ V/ms		5		150	us
	$dV_{CC}/dt \leq 30$ V/ms				2000	us
$t_{d(SVSon)}$	SVSon, switch from VLD=0 to VLD ≠ 0, V_{CC} = 3 V		20		150	us
t_{settle}	VLD ≠ 0 (Note 2)				12	us
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \leq 3$ V/s			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	$V_{CC}/dt \leq 3$ V/s	VLD = 1	70	120	155	mV
		VLD = 2 to 14	$V_{(SVS\_IT-)}$ x0.004		$V_{(SVS\_IT-)}$ x0.008	
	$V_{CC}/dt \leq 3$ V/s, external voltage applied to A7 terminal	VLD = 15	4.4		10.4	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \leq 3$ V/s	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61 (Note 1)	
		VLD = 13	3.24	3.5	3.76 (Note 1)	
		VLD = 14	3.43	3.7 (Note 1)	3.99 (Note 1)	
	$V_{CC}/dt \leq 3$ V/s, external voltage applied to A7 terminal	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (Note 3)	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	uA

Note:

1. The maximum operating voltage is 3.6V.

2. tsettle is the settle time that comparator needs to stabilize level when VLD switches from not 0 to the value between 2 and 15. The overdrive voltage is assumed to be more than 50mV.

3. The consumption current of SVS module has been included in Icc.

DCO

Parameter	Condition		Min	Typ	Max	Unit
$f_{(DCOCLK)}$	N(DCO)=01Eh, FN_8=FN_4=FN_3=FN_2=0,D=2; DCOPLUS = 1, $f_{Crystal}$=32.768kHz	VCC = 2.2 V/3V		1		MHz
$f_{(DCO=2)}$	FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1	VCC = 2.2 V	0.3	0.65	1.25	MHz
		VCC = 3 V	0.3	0.7	1.3	MHz
$f_{(DCO=2)}$	FN_8=FN_4=FN_3=0， FN_2=1; DCOPLUS = 1	VCC = 2.2 V	0.7	1.3	2.3	MHz
		VCC = 3 V	0.8	1.5	2.5	MHz
$f_{(DCO=2)}$	FN_8=FN_4=0,FN_3=1,FN_2=x; DCOPLUS = 1	VCC = 2.2 V	1.2	2	3	MHz
		VCC = 3 V	1.3	2.2	3.5	MHz
S_n	$S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	N(DCO) =01Eh, FN_8=FN_4=FN_3=FN_2=0, D= 2; DCOPLUS = 0	VCC = 2.2 V	-0.2	-0.3	-0.4	%/°C
		VCC = 3 V	-0.2	-0.3	-0.4	%/°C
D_V	N(DCO) =01Eh, FN_8=FN_4=FN_3=FN_2=0, D= 2; DCOPLUS = 0	VCC = 2.2 V/3V	0	5	15	%/V

MCU Crystal Oscillator, LFXT1 Oscillator (Note 1, 2)

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Integrated Input Capacitance	C_{XIN}	OSCCAPx = 0h	2.2 V/3 V		0		pF
		OSCCAPx = 1h	2.2 V/3 V		10		
		OSCCAPx = 2h	2.2 V/3 V		14		
		OSCCAPx = 3h	2.2 V/3 V		18		
Integrated Output Capacitance	C_{XOUT}	OSCCAPx = 0h	2.2 V/3 V		0		pF
		OSCCAPx = 1h	2.2 V/3 V		10		
		OSCCAPx = 2h	2.2 V/3 V		14		
		OSCCAPx = 3h	2.2 V/3 V		18		
Input Logic on XIN	V_{IL}	Note 3	2.2 V/3 V	VSS		0.2VCC	V
	V_{IH}			0.8VCC		VCC	V

Note:

1. The parasitic capacitance generated from package and board is about 2pF. The crystal effective load capacitance is (C_{XIN} x C_{XOUT})/(C_{XIN} + C_{XOUT}), which has nothing with XTS_FLL.

2. There are some principles to be observed as follows, in order to improve the EMI characteristic of low power dissipation LFXT1 oscillator, especially in LF mode(32kHz).

(1) The traces between the MS616F187 and crystal should be as short as possible.

(2) Optimal design of ground plane near oscillator pin.

(3) Avoid that other clock and data lines have crosstalk with XIN and XOUT pins.

(4) Avoid layout traces below or near XIN and XOUT pins.

(5) By using match materials and repeated practices to reduce parasitic load on XIN, XOUT pins.

(6) If use protection coating, pay attention not to cause capacitive and resistive leakage among oscillator pins.

3. Only valid when using external logic clock and must set XTS_FLL bit. While invalid when using crystal and resonator.

4. For accurate real time clock application, OSCCAPx=0h, apply recommended capacitance.

MCU Crystal Oscillator, XT2 Oscillator (Note 1)

Parameter		Condition	Min	Typ	Max	Unit
Integrated Input Capacitance	C_{XT2IN}	V_{CC} = 2.2 V/3 V		2		pF
Integrated Output Capacitance	C_{XT2OUT}	V_{CC} = 2.2 V/3 V		2		pF
Input Logic on XT2IN	V_{IL}	V_{CC} = 2.2 V/3 V	VSS		0.2VCC	V
	V_{IH}	Note 2	0.8VCC		VCC	V

Note: 1. The two terminals of oscillator all need to connect with load capacitance. The accurate capacitance value is provided by crystal manufacturer.

2. Only valid when using external logic clock and must set XTS_FLL bit. While invalid when using crystal and resonator.

MCU 中 USART0, USART1 (Note 1)

Parameter		Condition	Min	Typ	Max	Unit
USART0/1: Deglitch Time	t(τ)	V_{CC} = 2.2 V, SYNC = 0, UART mode	200	430	800	ns
		V_{CC} = 3 V, SYNC = 0, UART mode	150	280	500	

Note 1: The signal applied to USART0/1 receive terminal should meet t(τ) timing requirement, thus ensure URXS trigger is set. URXS trigger is set by low level pulse, which satisfies t(τ) minimum timing requirement. The operating conditions set by flag bit must be independent of the timing constraint. The deglitch circuit only operate when URXD0/1 line transmit negatively.

12-bit ADC, Power Supply and Input Range (Note 1)

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Analog Power Supply	AVCC	AVCC and DVCC is connected together, AVSS and DVSS is connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
Analog Input Voltage (Note 2)	$V_{(P6.x/Ax)}$	Applicable to all P6.0/A0 to P6.7/A7 terminals. Analog input terminal is selected by ADC12MCTLx and P6Sel.x=1,0 ≤ x ≤ 7; $V_{(AVSS)} \le V_{P6.x/Ax} \le V_{(AVCC)}$		0		V_{AVCC}	V
Operating Current on AV_{CC} (Note 3)	I_{ADC12}	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 1, REFON = 0 SHT0=0, SHT1=0, ADC12DIV=0	2.2V		0.65	1.3	mA
			3V		0.8	1.6	
Operating Current on AV_{CC} (Note 4)	I_{REF+}	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, REF2_5V = 1	3V		0.5	0.8	mA
		$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2V		0.5	0.8	mA
			3V		0.5	0.8	
Input Capacitance	C_I	Choose only one terminal, P6.x/Ax	2.2V			40	pF
Input Multiplexer Resistance	R_I	$0V \le V_{Ax} \le V_{AVCC}$	3V			2000	Ω

Note :

1. Leakage current has been defined in P.x/Ax terminal parameter sheet.
2. Analog input voltage range should be within reference voltage range, thus achieve valid conversion result.
3. Reference current is not included in I_{ADC12}.
4. Reference current is provided by AVCC. And the current is independent of ADC12ON until conversion starts. Before A/D conversion, set REFON bit to enable built-in reference voltage module.

12-bit ADC, External Reference

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Positive External Reference Voltage Input	V_{eREF+}	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (Note 2)		1.4		V_{AVCC}	V
Negative External Reference Voltage Input	V_{REF-}/V_{eREF-}	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (Note 3)		0		1.2	V
External Reference Differential Voltage Input	(V_{eREF+} - V_{REF-}/V_{eREF-})	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (Note 4)		1.4		V_{AVCC}	V
Static Input Current	I_{VeREF+}	$0V \le V_{eREF+} \le VAVCC$	2.2 V/3 V			±1	uA
Static Input Current	$I_{VREF-/VeREF-}$	$0V \le V_{eREF+} \le VAVCC$	2.2 V/3 V			±1	uA

Note :

1. External reference charges and discharge capacitance array during conversion.For external reference, input capacitance Ci is dynamic load during conversion period. The dynamic impedance of reference voltage should be matched with analog source impedance recommendation, achieving 12-bit setup accuracy on charging.
2. The accuracy constrains the minimum of positive external reference voltage. Decreasing accuracy demand could use lower reference voltage.
3. The accuracy constrains the maximum of negative external reference voltage. Decreasing accuracy demand could use higher reference voltage.
4. The accuracy constrains the difference of external reference voltage. Decreasing accuracy demand could use lower difference reference voltage.

12-bit ADC, Built-in Reference

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Positive Built-in Reference Voltage	V_{REF+}	REF2_5V = 1, $I_{VREF+} \le I_{VREF+}$max	3V	2.4	2.5	2.6	V
		REF2_5V = 0, $I_{VREF+} \le I_{VREF+}$max	2.2 V/3 V	1.44	1.5	1.56	
Minimum Power Supply of Positive Built-in Reference Voltage	$AVCC_{(min)}$	REF2_5V = 0, $I_{VREF+} \le$ 1mA		2.2			V
		REF2_5V = 1, $I_{VREF+} \le$ 0.5mA		V_{REF+} + 0.15			
		REF2_5V = 1, $I_{VREF+} \le$ 1mA		V_{REF+} + 0.15			
Load Current on V_{REF+}	I_{VREF+}		2.2 V	0.01		-0.5	mA
			3V			-1	
Load Modulation Current on V_{REF+}	$I_{L(VREF)+}$	I_{VREF+}= 500 uA +/− 100uA Analog input voltage~0.75V; REF2_5V = 0	2.2 V			±2	LSB
			3V			±2	LSB
		I_{VREF+} = 500 uA +/− 100uA Analog input voltage~1.25 V; REF2_5V = 1	3V			±2	LSB
Load Modulation Time on V_{REF+}	$I_{DL(VREF)+}$	I_{VREF+}=100 uA → 900uA, C_{VREF+} = 5 µF, Analog input voltage~ 0.5V_{REF+} Conversion result error≤ 1 LSB	3V			20	ns
External Capacitance on V_{REF+} (Note 1)	C_{VREF+}	REFON =1, 0 mA ≤ I_{VREF+} ≤ I_{VREF+}max	2.2 V/3 V	5	10		uF
Temperature Coefficient of Built-in Reference	T_{REF+}	I_{VREF+} is a constant, range: 0mA ≤ I_{VREF+} ≤ 1mA	2.2 V/3 V			±100	ppm/ °C
Setup Time of Built-in Reference (Note 2)	t_{REFON}	I_{VREF+}= 0.5mA, C_{VREF+} = 10µF, V_{REF+} = 1.5 V	2.2 V			17	ms

Note :

1. Internal buffer magnifier and accuracy demand need one external capacitor. For all INL and DNL tests, connect two capacitors between V_{REF+} and A_{VSS}, V_{REF-}/V_{eREF-} and AV_{SS}, a 10uF tantalum capacitor and a 100nF ceramic capacitor.

2. Test condition: the conversion error is less than ±0.5 LSB after t_{REFON} opens. The setup time is up to external capacitance load.

12-bit ADC, Timing Parameter

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
$f_{ADC12CLK}$		Ensure accuracy of ADC linearity parameter	2.2V/3 V	0.45	5	6.3	MHz
Internal ADC12 Oscillator	$f_{ADC12OSC}$	ADC12DIV=0, $f_{ADC12CLK}=f_{ADC12OSC}$	2.2 V/ 3 V	3.7		6.3	MHz
Conversion Time	$t_{CONVERT}$	C_{VREF+} ≥ 5uF, internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz - 6.3 MHz	2.2 V/ 3 V	2.06		3.51	us
		External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK: ADC12SSEL ≠ 0			13·ADC12DIV·1/$f_{ADC12CLK}$		us
ADC Enable Time	$t_{ADC12ON}$	Note 1				100	ns
Sampling Time	t_{Sample}	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, τ= [R_S + R_I] x C_I;(Note 2)	3V	1220			ns
			2.2V	1400			

Note :

1. After ADC12ON is enabled, $t_{ADC12ON}$ is the time when the conversion error is less than ±0.5 LSB. And the reference voltage and input signal have be set.

2. After about 10τ, the conversion error is less than ±0.5 LSB, $t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800ns$ (n=ADC resolution=12, RS= input resistance).

12-bit ADC, Linearity Parameter

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Integral Nonlinearity Error	E_I	1.4 V ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}) min ≤ 1.6 V	2.2 V/ 3 V			±2	LSB
		1.6 V < (V_{eREF+} − V_{REF-}/V_{eREF-}) min ≤ [$V_{(AVCC)}$]				±1.7	
Differential Nonlinearity Error	E_D	(V_{eREF+} − V_{REF-}/V_{eREF-}) min ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 uF (tantalum) and 100 nF (ceramic)	2.2 V/ 3 V			±1	LSB
Offset Error	E_O	(V_{eREF+} − V_{REF-}/V_{eREF-}) min ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), Internal impedance of source R_S < 100Ω, C_{VREF+} = 10 uF (tantalum) and 100 nF (ceramic)	2.2 V/ 3 V		±2	±4	LSB
Gain Error	E_G	(V_{eREF+} − V_{REF-}/V_{eREF-}) min ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 uF (tantalum) and 100 nF (ceramic)	2.2 V/ 3 V		±1.1	±2	LSB
Total Unadjusted Error	E_T	(V_{eREF+} − V_{REF-}/V_{eREF-}) min ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 uF (tantalum) and 100 nF (ceramic)	2.2 V/ 3 V		±2	±5	LSB

12-bit ADC, Temperature Sensor and Built-in Mid-voltage VMID

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Current on AV_{CC} (Note 1)	I_{SENSOR}	REFON = 0, INCH = 0Ah, ADC12ON=NA, T_A = 25	2.2 V		40	120	uA
			3 V		60	160	
V_{SENSOR}		ADC12ON =1, INCH = 0Ah,T_A =0°C	2.2 V		986	986±5%	mV
			3 V		986	986±5%	
TC_{SENSOR}		ADC12ON = 1, INCH = 0Ah	2.2 V		3.55	3.55±3%	mV/°C
			3 V		3.55	3.55±3%	
Sampling Time Required by Selecting Channel 10 (Note 2)	$t_{sensor(sample)}$	ADC12ON = 1, INCH = 0Ah, Conversion error ≤ 1 LSB	2.2 V	30			us
			3 V	30			
Current Divided on Channel 11	I_{VMID}	ADC12ON = 1, INCH = 0Bh, (Note 3)	2.2 V			NA	uA
			3 V			NA	
Voltage Divided on Channel 11	V_{MID}	ADC12ON = 1, INCH = 0Bh, V_{MID} is~0.5 x V_{AVCC}	2.2 V		1.1	1.1±0.04	V
			3 V		1.5	1.5±0.04	
Sampling Time Required by Selecting Channel 11	$t_{VMID(sample)}$	ADC12ON = 1, INCH = 0Bh, Conversion error≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

Note :

1. If (ADC12ON=1, REFON=1) or (ADC12ON=1, INCH=0Ah and sampling signal at high-level), sensor current I_{SENSOR} would be generated. The current includes the values through senor and reference.
2. Typical equivalent impedance of sensor is 51kΩ. The sampling time includes sensor enabled time $t_{SENSOR(on)}$.
3. V_{MID} is only used during sampling process, without generating extra current.
4. The sampling time, $t_{VMID(sample)}$ has included enabled time $t_{VMID(on)}$, without extra time.

Flash

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Operating Voltage at Programming, Erasing	$V_{CC(PGM/ERASE)}$			2.7		3.6	V
The Frequency for Flash Programming Timing	f_{FTGP}			257		476	kHz
The Frequency for Flash Erasing Timing	f_{FTGE}			15		100	kHz
Current on DVCC at Programming	I_{PGM}		2.7 V/ 3.6 V		3	5	mA
Current on DVCC at Erasing	I_{ERASE}		2.7 V/ 3.6 V		3	7	mA
Accumulated Programming Time	t_{CPT}	Note 1	2.7 V/ 3.6 V			10	ms

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Accumulated Large-scale Erasing Time	$t_{CMErase}$	Note 2	2.7 V/ 3.6 V	200			ms
Programming/ Erasing Duration				10^4	10^5		cycles
Data Save Cycle	$t_{Retention}$	T_J = 25°C		100			years
Word Programming Time	t_{Word}	Note 3			35		t_{FTG}
Block Programming Time of the First Word	$t_{Block, 0}$				30		
Block Programming Time of Each Additional Word	$t_{Block, 1-63}$				21		
Waiting Time for Block Programming Finishing Sequencing	$t_{Block, End}$				6		
Large-scale Erasing Time	$t_{Mass Erase}$				5297		
Segment Erasing Time	$t_{Seg Erase}$				4819		

Note：

1. When a 64-bit Flash module is written, it couldn't exceed accumulated programming time.The parameter is applicable to all Flash programming methods.
2. The large-scale erasing time is up to Flash timing.
   At least 11.1ms (= 5297x1/f_{FTG}, maximum = 5297x1/476kHz).
3. These values have been fixed into the state machine of Flash controller.
4. The erasing frequency on chip is less than 100K.
5. Program on chip by word format, rather than byte format.
6. Information storage only has A segment (128 bytes), without B segment.
7. 2048 bytes rather than 512 bytes in each segment of master storage.

JTAG, Interface

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
TCK Input Frequency	f_{TCK}	Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
Internal Pull-up Resistors on TMS, TCK, TDI/TCLK	$R_{Internal}$	Note 2	2.2 V/ 3 V	25	60	90	kΩ

Note :

1. f_{TCK} may be constrained by the timing requirement of selected module.
2. TMS, TDI/TCLK and TCK pull-up resistors have been integrated.

JTAG, Fuse (Note 1)

Parameter		Condition	Min	Typ	Max	Unit
Power Supply Needed by Fuse-blow	$V_{CC(FB)}$	T_A = 25°C	2.5			V
TDI/TCLK Voltage Needed by Fuse-blow	V_{FB}		6		7	V

Parameter		Condition	Min	Typ	Max	Unit
TDI/TCLK Current Needed by Fuse-blow	I_{FB}				100	mA
Time for Fuse-blow	t_{FB}				1	ms

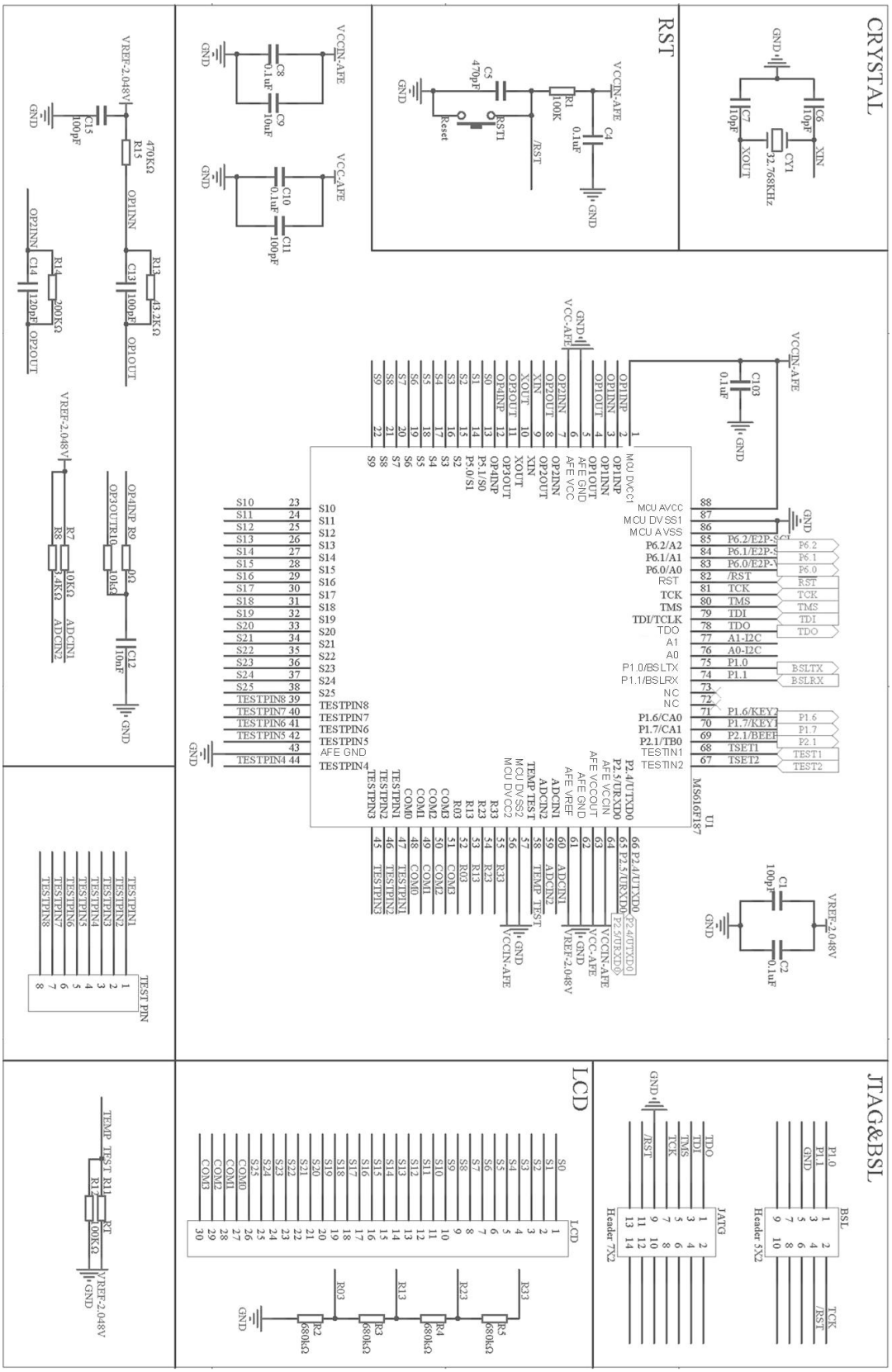
Note 1: Once the fuse is blown, the JTAG/Test of the MS616F187 can't be connected, and the simulation characteristic would be lost. JTAG mode is switched to bypass mode.

AFE Electrical Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Reference					
Reference Output Voltage		2.043	2.048	2.053	V
System					
Resolution and No Missing Resolution	DR=00	12		12	Bits
	DR=01	13		13	Bits
	DR=10	15		15	Bits
	DR=11	16		16	Bits
Output Rate	DR=00		480		SPS
	DR=01		240		SPS
	DR=10		60		SPS
	DR=11		30		SPS
Integral Nonlinearity Error	DR=11,PGA=1,End Point		±0.004	±0.010	% of FSR(2)
Offset Error	PGA=1		3.9	8	mV
	PGA=2		3.8	5	mV
	PGA=4		3.8	4.5	mV
	PGA=8		3.5	4.5	mV
Operational Amplifier					
Input Offset Voltage	-0.3V<VCM<+3.5V		0.4	1	mV
	-40°C≤TA≤125°C			1	
Input Bias Current	-40°C≤TA≤125°C		0.2	1	pA
	-40°C≤TA≤125°C			110	pA
	-40°C≤TA≤125°C			780	pA
Input Offset Current	-40°C≤TA≤125°C		0.1	0.5	pA
	-40°C≤TA≤125°C			50	pA
	-40°C≤TA≤125°C			250	pA
Common-mode Rejection Ratio	0V<VCM<+3.5V		75		dB
	-40°C≤TA≤125°C	68			
Large Signal Gain	RL=10kΩ, Vo=0.5V~4.5V	100	105		dB
Input Offset Voltage Drift	-40°C≤TA≤125°C		5	10	μV/°C

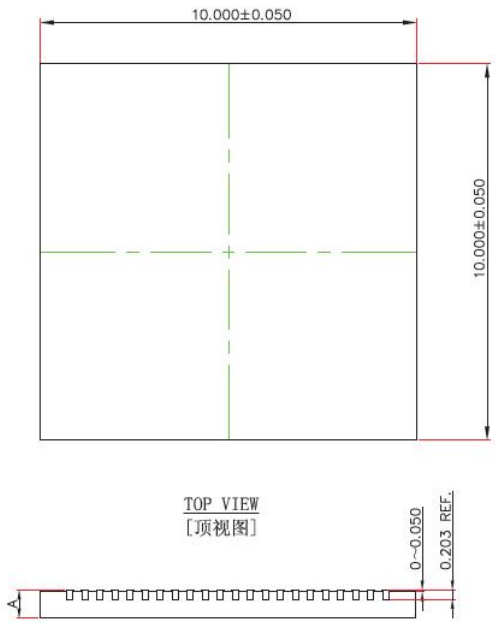
Parameter	Condition	Min	Typ	Max	Unit
Input Capacitance	C_{DIFF}		1.9		pF
	C_{CM}		2.5		pF
Output High-level Voltage	IL=1mA	4.95	4.98		V
	-40°C≤TA≤125°C	4.9			
	IL=10mA		4.7		V
	-40°C≤TA≤125°C	4.50			
Output Low-level Voltage	IL=1mA		20	30	mV
	-40°C≤TA≤125°C			50	
	IL=10mA		190	275	mV
	-40°C≤TA≤125°C			335	
Short-circuit Current			±80		mA
Closed-loop Output Impedance	f=10kHZ, AV=1		15		Ω
Power Supply Rejection Ratio	1.8V<VCM<+3.5V	67	90		dB
	-40°C≤TA≤125°C	64			dB
Static Current	Vo=Vs/2		40		μA
	-40°C≤TA≤125°C			50	
Gain Bandwidth Product	RL=100kΩ		0.4		MHz
	RL=10kΩ		0.4		MHz
Slew Rate	RL=10kΩ		0.3		V/μs
Setup Time 0.1%	G=±1,2Vstep CL=20pF,RL=1kΩ		23		us
Phase Margin	RL=100kΩ,RL=10kΩ,CL=20pF		65		Deg
Peak-to-Peak Noise			2.3	3.5	uV
Voltage Noise Density	f=1kHZ		26		$nV/\sqrt{Hz}$
	f=10kHZ		24		$nV/\sqrt{Hz}$
Current Noise Density	f=1kHZ		0.05		$pA/\sqrt{Hz}$
Digital Input/ Output					
Input High-level Voltage		0.7·VA		3.6	V
Input Low-level Voltage		GND-0.5		0.3·VDD	V
Output Low-level Voltage	I_{OL}=3mA	GND		0.4	V
Input High-level Peak Current				10	uA
Input Low-level Peak Current		-10			uA
Power Supply					
Operating Voltage	VDD	2.5		3.6	V
Power Supply Current	Off State		0.05	2	uA
	Operation State		1400	1600	uA

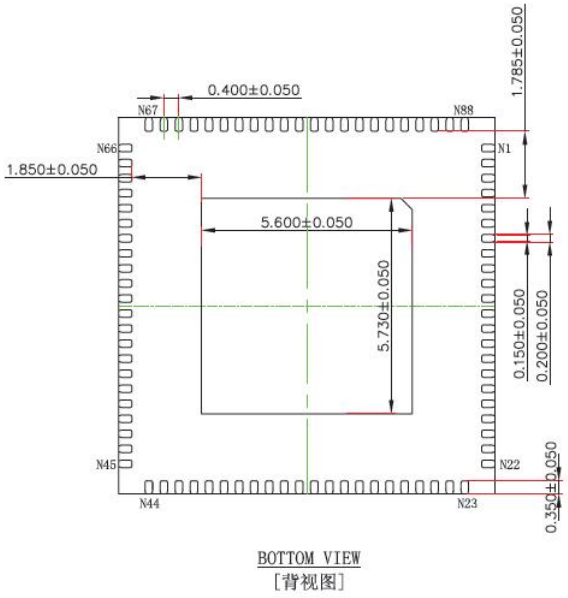
TYPICAL APPLICATION DIAGRAM



PACKAGE OUTLINE DIMENSIONS

QFN88





	MIN.	NORM.	MAX.
A	0.700	0.750	0.800
	0.800	0.850	0.900

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name：MS616F187

Product Code： XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Tray	Tray/Box	Piece /Box	Box/Carton	Piece/Carton
MS616F187	QFN88	168	10	1680	4	6720

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- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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