2.7V to 5.5V, 12Bit, Optional Built-in Reference, Four-Channel DAC

PRODUCT DESCRIPTION

The MS5814/MS5814T is a 12bit, four-channel output voltage DAC with optional internal reference. The interface uses four-wire serial port mode or I^2C interface. The MS5814/MS5814T has 16bit control data, including DAC address, control byte and 12bit DAC data. The power supply range is 2.7V to 5.5V. The output of resistor string is connected to a class AB, rail-to-rail output buffer with 6dB gain. The MS5814/MS5814T integrates power-down mode to reduce power dissipation.

The MS5814 is available in SOP16 package and the MS5814T is available in TSSOP16 package.

SOP16

TSSOP16

FEATURES

- 12bit Accuracy
- Programmable Setup Time: 3μs or 9μs
- Built-in Optional 1.5V, 2.5V Reference
- Four-Wire Serial Port Mode or I^2C Interface
- Internal Power on Reset
- Low Power Dissipation: 10mW, 5V (Slow Mode)
  4.2mW, 3V (Slow Mode)
- Integrated REF Buffer
- Output Range: Twice the Reference Voltage
- Software, Hardware Power Down
- Power Supply: 2.7V~5.5V

APPLICATIONS

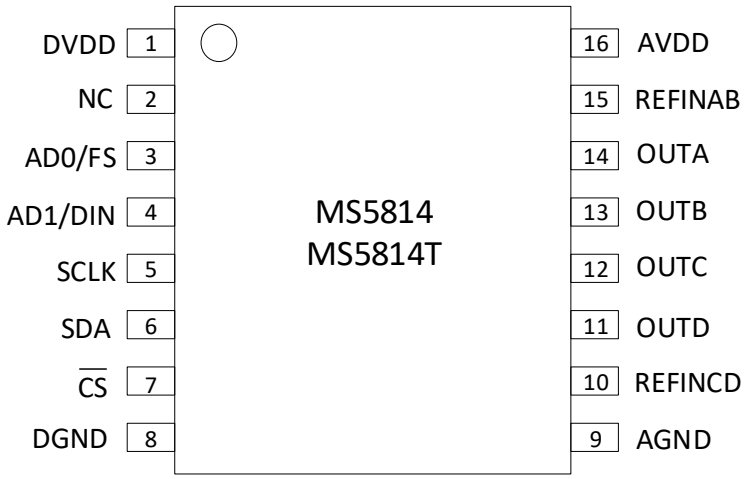
- Digital Servo System Control
- Digital Compensation and Gain Adjustment
- Industrial Process Control
- Mechanical and Mobile Control Equipment
- High-capacity Storage Device

PRODUCT SPECIFICATION

Part Number	Package	Marking
*MS5814	SOP16	MS5814
MS5814T	TSSOP16	MS5814T

* The package is not available temporarily. If necessary, please contact Hangzhou Ruimeng Sales Department Center.

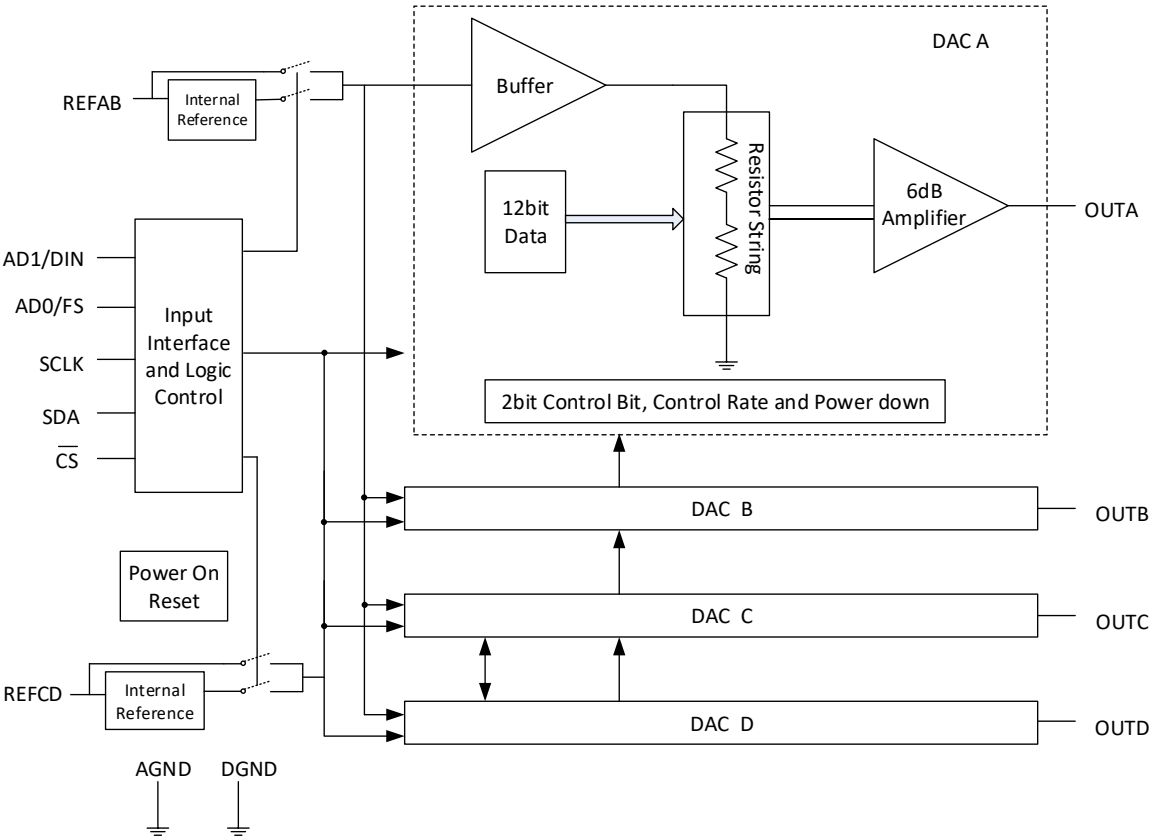
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	DVDD	-	Digital Power Supply
2	NC	-	Not Connection
3	AD0/FS	I	I^2C Address AD0 / Frame Synchronization for SPI Interface
4	AD1/DIN	I	I^2C Address AD1 / Data Input for SPI Interface
5	SCLK	I	Serial Digital Clock Input
6	SDA	I/O	I^2C Data Input/Output
7	$\overline{CS}$	I	SPI Interface Chip Select, Active Low
8	DGND	-	Digital Ground
9	AGND	-	Analog Ground
10	REFINCD	I	Reference Input Voltage for Channel C and D, Optional for Internal Reference or External Reference
11	OUTD	O	Analog Output for Channel D
12	OUTC	O	Analog Output for Channel C
13	OUTB	O	Analog Output for Channel B
14	OUTA	O	Analog Output for Channel A
15	REFINAB	I	Reference Input Voltage for Channel A and B, Optional for Internal Reference or External Reference
16	AVDD	-	Analog Power Supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Analog Power Supply	AVDD	-0.3 ~ +7	V
Digital Power Supply	DVDD	-0.3 ~ +7	V
Power Supply Difference	AVDD to DVDD	-2.8 ~ +2.8	V
Input Digital Voltage Range	V_{IN}	-0.3 ~ DVDD+0.3	V
Reference Input Voltage Range	V_{REFIN}	-0.3 ~ AVDD+0.3	V
Operating Temperature Range	T_A	-40 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C
Maximum Junction Temperature	J_T	150	°C
Lead Temperature (10s)		260	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Condition	Min	Typ	Max	Unit
Power Supply	5V Power Supply	4.5	5	5.5	V
	3V Power Supply	2.7	3	3.3	
High-level Digital Input Voltage (V_{IH})	DVDD = 2.7V	2			V
	DVDD = 5.5V	2.4			
Low-level Digital Input Voltage(V_{IL})	DVDD = 2.7V			0.6	V
	DVDD = 5.5V			1	
Reference Voltage	5V Power Supply (See Note 1)	0	2.048	AVDD-1.5	V
	3V Power Supply (See Note 1)	0	1.024	AVDD-1.5	
Load Resistance		2	10		kΩ
Load Capacitance				100	pF
SCLK Rate				20	MHz

Note 1: The input voltage greater than AVDD/2 will cause output saturation at large DAC input codes.

ELECTRICAL CHARACTERISTICS

Static DAC Parameters

Parameter		Condition	Min	Typ	Max	Unit
Resolution			12			Bits
Integral Non-linearity (INL)		See Note 2		±4		LSB
Differential Non-linearity (DNL)		See Note 3		±0.5	±1	LSB
Zero Point Offset		See Note 4			±10	mV
Zero Point Offset Temperature Drift		See Note 5		4.5		ppm/°C
Gain Error		See Note 6			±0.6	%of FS Voltage
Gain Error Temperature Drift		See Note 7		6		ppm/°C
PSRR	Zero Point	See Note 8 and Note 9		-65		dB
	Full-scale			-65		dB

Note: 2. Integral non-linearity (INL) refers to linearity error, which is the maximum deviation relative to ideal output, excluding zero point error and full-scale error.

3. Differential non-linearity (DNL) refers to differential error, which refers to the maximum amplitude change adjacent to LSB.

4. Zero point offset is the analog output when the digital input is zero.

5. Zero point offset temperature drift refers to the variation of analog output with temperature when the digital input is zero.

6. Gain error refers to the deviation between analog output and ideal output, excluding zero point offset.

7. Gain error temperature drift refers to the variation of the deviation between analog output and ideal output with temperature, excluding zero point offset.

8. Zero point power supply rejection ratio is the output change ratio caused by 5 ± 0.5 V and 3 ± 0.3V in AVDD when the digital inputs are all zero.

9. Full-scale output power supply rejection ratio is the output change ratio caused by 5 ± 0.5 V and 3 ± 0.3V in AVDD when the digital inputs are high.

DAC Output Parameters

Parameter	Condition	Min	Typ	Max	Unit
Output Voltage	R_L=10kΩ	0		AVDD-0.4	V
Output Load Adjustment Accuracy	R_L=2kΩ to 10kΩ		0.1	0.25	% of FS

Internal Reference Voltage Output Parameters

Parameter	Condition	Min	Typ	Max	Unit
Output Voltage	1.5V@25°C		1.5		V
	2.5V@25°C		2.5		

Parameter	Condition	Min	Typ	Max	Unit
Output Current			±400		μA
Temperature Drift			±6		ppm/°C
Start Setup Time	C(REF) =10μF		20		ms

Reference Input Voltage Parameters

Parameter	Condition		Min	Typ	Max	Unit
Input Voltage Range	See Note 10		0		AVDD-1.5	V
Input Resistance				7		MΩ
Input Capacitance						pF
Reference Feed Through	REFIN = 1Vpp(1 kHz) + 1.024 V (See Note 11)			-75		dB
Reference Input Bandwidth	REFIN = 0.2Vpp+1.024 V (Large Signal)	Slow		0.9		MHz
		Fast		1.8		

Note: 10. When reference input voltage exceeds VDD/2, saturation distortion will occur.

11. Reference feed through refers to the analog output rejection ratio when the output digits are all zero and REFIN = 1Vpp(1 kHz)+1.024V.

Digital Output Parameters

Parameter	Condition	Min	Typ	Max	Unit
High-level Digital Input Current	V_I=VDD			±1	μA
Low-level Digital input Current	V_I=0V			±1	μA
Input Capacitance			3		pF

Power Dissipation Parameters

Parameter	Condition		Min	Typ	Max	Unit
Power Supply Current	5V Power Supply, No Load, Plus CLOCK, All inputs are connected to 0V or VDD.	Slow		2.0	2.7	mA
		Fast		5.2	6	
	3V Power Supply, No Load, Plus CLOCK, All inputs are connected to 0V or VDD.	Slow		1.4	1.6	mA
		Fast		3.8	4.8	
Power Down Supply Current				10		nA

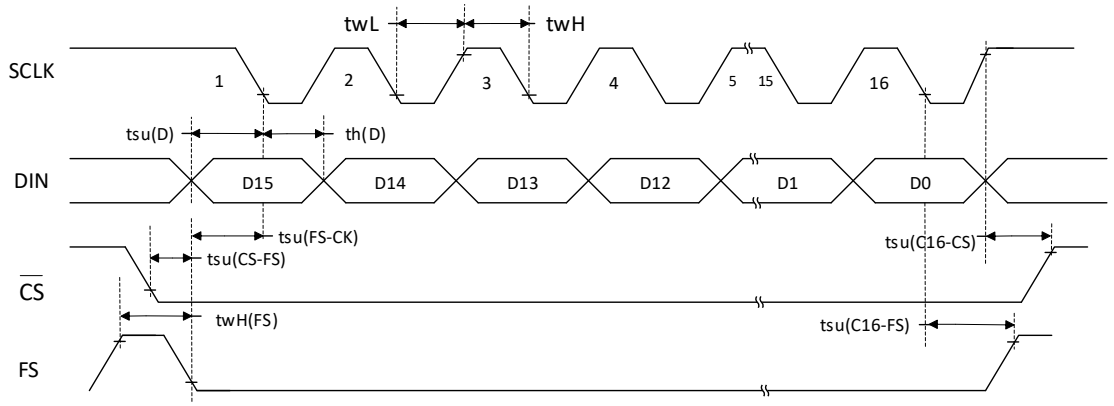
Analog Output Dynamic Parameters

Parameter	Condition		Min	Typ	Max	Unit
SR	C_L=100pF, R_L=10kΩ, V_O=10% to 90%, V_{REF}=2.048, 1.024	Fast		6.5		V/μs
		Slow		3.5		
		Slow		3.5	20	
Ts(c)	To ±0.5LSB, C_L=100pF, R_L=10KΩ	Fast		1		μs
		Slow		2		
Glitch Energy	From 7FF to 800			10		nV-sec
SNR	V_{REF}=1.024 at 3V; V_{REF}=2.048 at 5V, f_S=400kSPS, f_{OUT}=1.1kHz Sinewave, C_L=100pF, R_L=10kΩ, BW=20kHz			70		dB
S/(N+D)				65		
THD				-65		
SFDR				68		

Control Port -SPI Mode

Parameter	Condition	Min	Typ	Max	Unit
tsu(CS–FS)	Time from $\overline{CS}$ Low to FS Falling Edge	10			ns
tsu(FS–CK)	Setup Time from FS to the First SCLK Falling Edge	8			ns
tsu(C16–FS) of FS	Setup Time from the 16th SCLK Falling Edge of Sampling Data D0 to FS High	10			ns
tsu(C16–CS)	The 16th SCLK of Sampling Data D0 Stops (Setup Time from the Next Rising Edge to $\overline{CS}$ High)	10			ns
twH	SCLK High-level Width	25			ns
twL	SCLK Low-level Width	25			ns
tsu(D)	Data Setup Time before SCLK Falling Edge	8			ns
th(D)	Data Hold Time after SCLK Falling Edge	5			ns
twH(FS)	FS High Pulse Width	20			ns

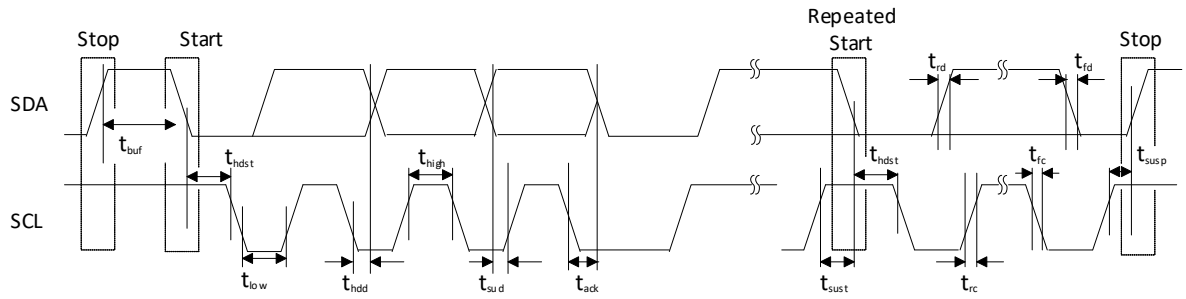
SPI Timing Diagram



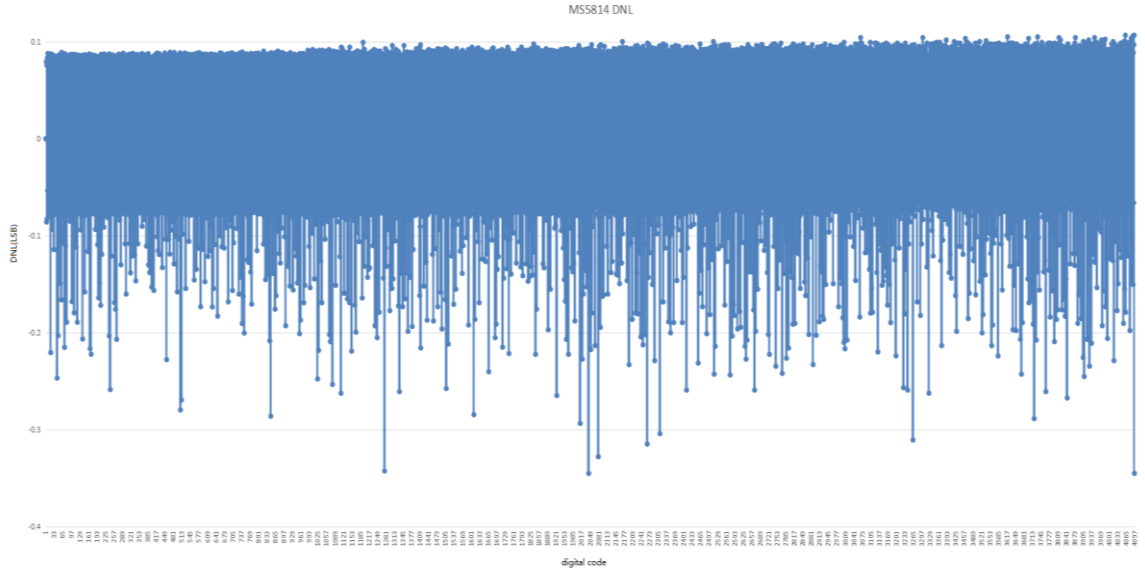
Control Port -I²C Mode

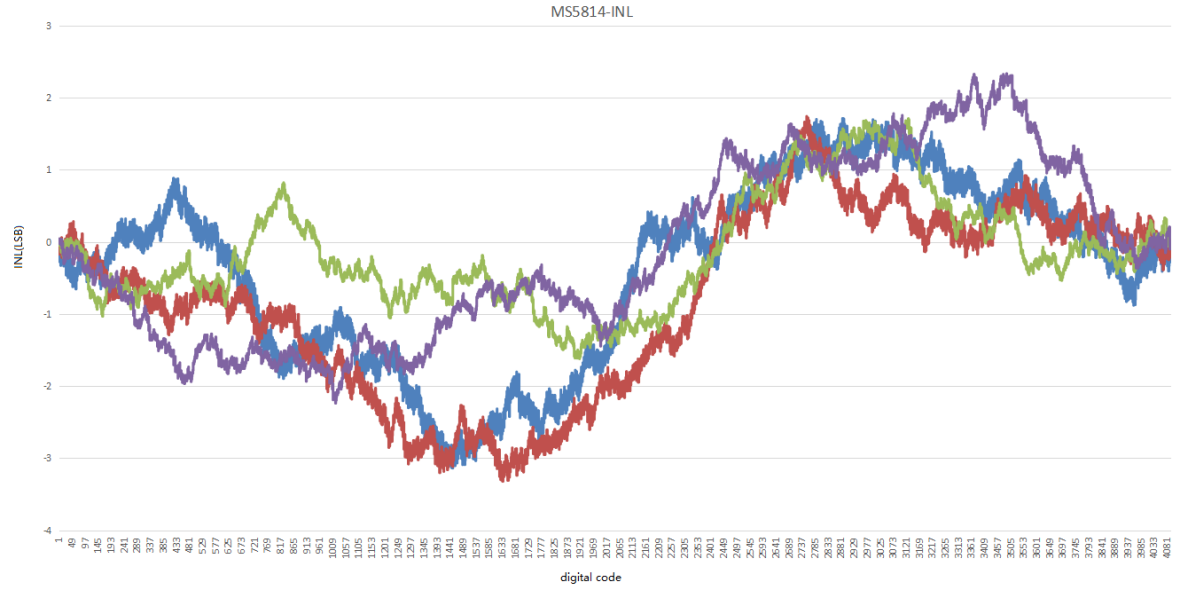
Parameter	Symbol	Min	Max	Unit
SCLK Clock Frequency	f_{scl}	-	100	kHz
Bus Free Time during Conversion	t_{buf}	4.7	-	µs
Start Condition Hold Time (before the First Clock Pulse)	t_{hdst}	4.0	-	µs
Low-level Clock Time	t_{low}	4.7	-	µs
High-level Clock Time	t_{high}	4.0	-	µs
Setup Time of Repeated Start Condition	t_{sust}	4.7	-	µs
Hold Time from SCL Falling Edge to SDA	t_{hdd}	10	-	ns
Setup Time from SDA to SCL Rising Edge	t_{sud}	250	-	ns
Rising Time of SCL and SDA	t_{rc} , t_{rd}	-	1000	ns
Falling Time of SCL and SDA	t_{fc}, t_{fd}	-	300	ns
Setup Time of Stop Condition	t_{susp}	4.7	-	µs
Delay from SCL Falling Edge to Acknowledge	t_{ack}	300	1000	ns

I²C Timing Diagram



TYPICAL CHARACTERISTICS CURVE





FUNCTION DESCRIPTION

General Function

The MS5814/MS5814T is a 12bit single power supply DAC with internal optional reference, whose structure is resistor string. And it integrates serial interface, rate and power down logic control, a reference input buffer, a resistor string and a rail-to-rail output amplifier.

The output voltage can be expressed as:

$$V_{OUT}=2x\frac{V_{REF}xD}{2^{12}}$$

Reference Voltage

The MS5814/MS5814T can choose internal or external reference through the internal register setting. The 1.5V and 2.5V can be chosen by internal reference. Please refer to register description for more details.

Be aware that when there is a requirement for full-scale output, the selection of reference voltage should meet the following requirements:

$$V_{REF}x2 \leq AVDD\text{-}200mV$$

Serial Interface

The MS5814/MS5814T integrates optional I^2C and SPI multiplexing interfaces. As a slave device, there are two modes in control port: SPI and I^2C. If there is a transition from high to low on the AD0/FS pin, SPI mode is selected. Connecting a resistor to DVDD or DGND on the AD0/FS pin, I^2C mode is selected. So the needed AD0 bit address state is fixed.

The MS5814/MS5814T is only valid when the $\overline{CS}$ is set low, then starts bit-wise data output at the FS falling edge(High active at the beginning), internal DAC updates corresponding output level when 16bits are all transferred or FS becomes high.

The MS5814/MS5814T serial port can adopt two basic modes: four-wire(using chip select $\overline{CS}$) and three-wire(not using chip select $\overline{CS}$), using chip selects can make many devices connected to data source for serial port(DSP or MCU).

I^2C Data Format

In I^2C mode, SDA is a bidirectional data line. Data inputs and outputs through a SCLK clock. There is no FS pin at this time. Pins AD0 and AD1 form two LSBs of chip address and a 20kΩ resistor should be connected to DVDD or DGND.

Figure 1 and 2 respectively show the signal timing for one write and one read cycles. When the clock signal is high, SDA has a falling shift as the start condition. When the clock signal is high, SDA has a rising shift as the stop condition. All other SDA transitions occur when the clock signal is low. After the start condition, the first byte consisting of 7-bit chip address and 1 read/write bit (high: read, low: write)is sent to the MS5814/MS5814T. The top 5 bits of the 7-bit address is the fixed 00100.

In the MS5814/MS5814T communication, chip address as the first byte is sent to the MS5814/MS5814T, and matches the AD1 and AD0 pins after 00100. The 8th address is the read/write bit. If it is a write operation,

the next byte includes the register address pointer (MAP), which is used to choose the register to read or write. If it is a read operation, the register referred to by the MAP will be output. MAP automatically increases, the register data will appear in sequence. Each byte is separated by a acknowledge bit (ACK). After reading the input bytes, the MS5814/MS5814T outputs the acknowledge bit. After transmitting each byte, micro-controller sends the acknowledge bit to the MS5814/MS5814T.

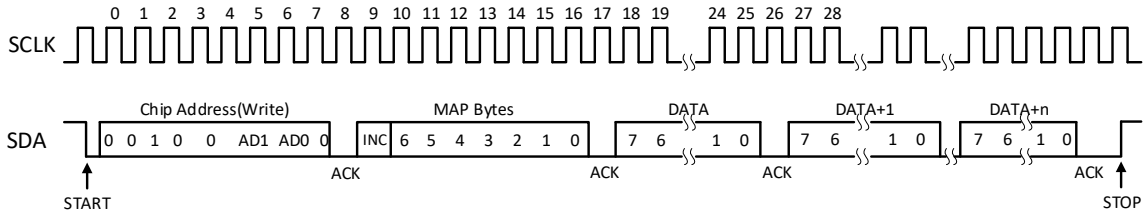


Figure 1. Control Port Timing, I²C Slave Mode Write

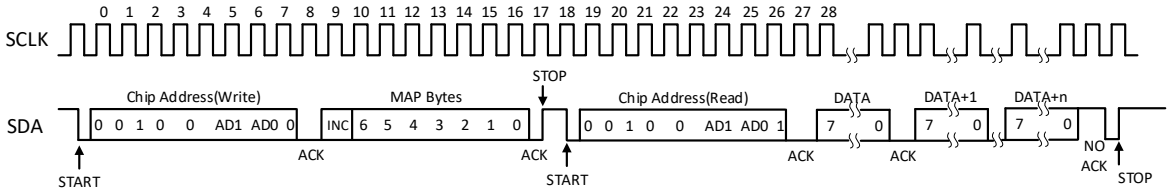


Figure 2. Control Port Timing, I²C Slave Mode Read

Be aware that MAP cannot be set in read operation, so a suspend write operation is needed as a header code. As shown in Figure 2, after sending a stop condition as an acknowledgement to MAP, the write operation stops.

I²C Register Address Pointer (MAP)

The MAP has an 8-digit word length. It includes the control port address that can be read and write in I²C mode. In addition, it has an automatic increment control bit. The MAP[6:0] consists address that can be read and write, the seventh bit (INC) determines whether the MAP[6:0] automatically increase after each control port completes. If INC=0, MAP[6:0] will not automatically increase after completing read or write on each control port, if INC=1, MAP[6:0] will automatically increase after completing read or write on each control port. The MAP bits are shown in Figure 1 or 2.

I²C Register

Address	7	6	5	4	3	2	1	0
01h	A1	A0	LDAC	Reserved	D11	D10	D9	D8
	0	0	0	0	0	0	0	0
02h	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0
03h	SPD	REFSEL	REFABSEL	REFCDSEL	OUT_CA	OUT_CB	OUT_CC	OUT_CD
	0	0	0	0	0	0	0	0

A1, A0: Internal DAC Channel Address Selection Bit

LDAC: 1, Update data input register for present address, but not update DAC register;

0, Update to output simultaneously based on the four present DAC registers;

D11-D0: Internal DAC Data

SPD: Rate Control, 1: Fast Mode, 0: Slow Mode;

REFSEL: Internal Reference Selection, 1: Select 2.5V, 0: Select 1.5V;

REFABSEL: A, B Channel Reference Selection, 1: Select Internal Reference, 0: Select External Reference;

REFCDSEL: C, D Channel Reference Selection, 1: Select Internal Reference, 0: Select External Reference;

OUT_CA: Output State of Control A Channel, 1: High-impedance State Output, 0: Normal Output(Output impedance to the ground is about 120kΩ);

OUT_CB: Output State of Control B Channel, 1: High-impedance State Output, 0: Normal Output(Output impedance to the ground is about 120kΩ);

OUT_CC: Output State of Control C Channel, 1: High-impedance State Output, 0: Normal Output(Output impedance to the ground is about 120kΩ);

OUT_CD: Output State of Control D Channel, 1: High-impedance State Output, 0: Normal Output(Output impedance to the ground is about 120kΩ);

Note: When OUT_CA, OUT_CB, OUT_CC and OUT_CD are 1, the chip is in power down mode.

SPI Data Format

The SPI data of the MS5814/MS5814T includes two formats: configuration register format and data register format.

Configuration Register Format

MSB LSB

X	X	X	1	SPD	REFSEL	REFABSEL	REFCDSEL	OUT_CA	OUT_CB	OUT_CC	OUT_CD	X	X	X	X

X: Represent Both High-level and Low-level;

SPD: Rate Control, 1: Fast Mode, 0: Slow Mode;

REFSEL: Internal Reference Selection, 1: Select 2.5V, 0: Select 1.5V;

REFABSEL: A, B Channel Reference Selection, 1: Select Internal Reference, 0: Select External Reference;

REFCDSEL: C, D Channel Reference Selection, 1: Select Internal Reference, 0: Select External Reference;

OUT_CA: Output State of Control A Channel, 1: High-impedance State Output, 0: Normal Output(Output impedance to the ground is about 120kΩ);

OUT_CB: Output State of Control B Channel, 1: High-impedance State Output, 0: Normal Output(Output impedance to the ground is about 120kΩ);

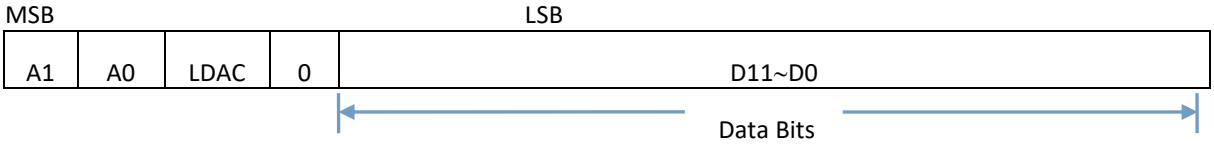
OUT_CC: Output State of Control C Channel, 1: High-impedance State Output, 0: Normal Output(Output impedance to the ground is about 120kΩ);

OUT_CD: Output State of Control D Channel, 1: High-impedance State Output, 0: Normal Output(Output impedance to the ground is about 120kΩ);

Note: When OUT_CA, OUT_CB, OUT_CC and OUT_CD are 1, the chip is in power down mode.

Data Register Format

Data register consists of two parts: control bits (D15~D12) and digital data (D11~D0).



LDAC: 1, Update data input register for present address, but not update DAC register;

0, Update to output simultaneously based on the four present DAC registers;

A1 and A0 are internal DAC channel address selection bits, the truth table is as follows:

A1	A0	DAC Address
0	0	DAC-A
0	1	DAC-B
1	0	DAC-C
1	1	DAC-D

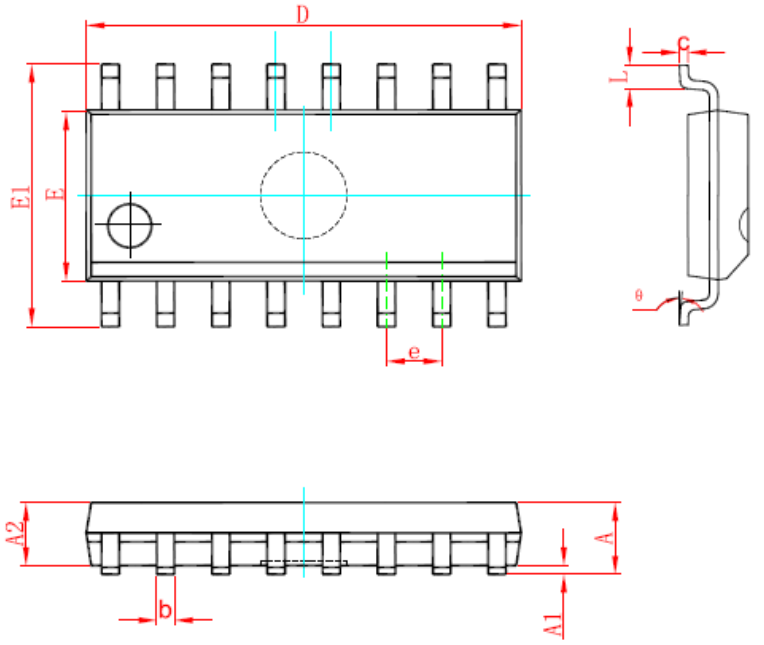
Power Supply Bypass and Ground Management

To improve system performance, when in PCB design, it is necessary to connect analog ground and digital ground respectively to different ground connection layers, the two ground surfaces should be connected together at the low impedance nodes of the system. It is better to connect the AGND of the DAC to the analog ground of the system, making sure that analog ground current can be well managed and the voltage drop of the analog ground connection line can be ignored.

The 0.1μF ceramic decoupling capacitance can be connected between the chip power supply and ground and be placed as close to the chip as possible. Using magnetic rings can further separate the system analog supplies and digital supplies.

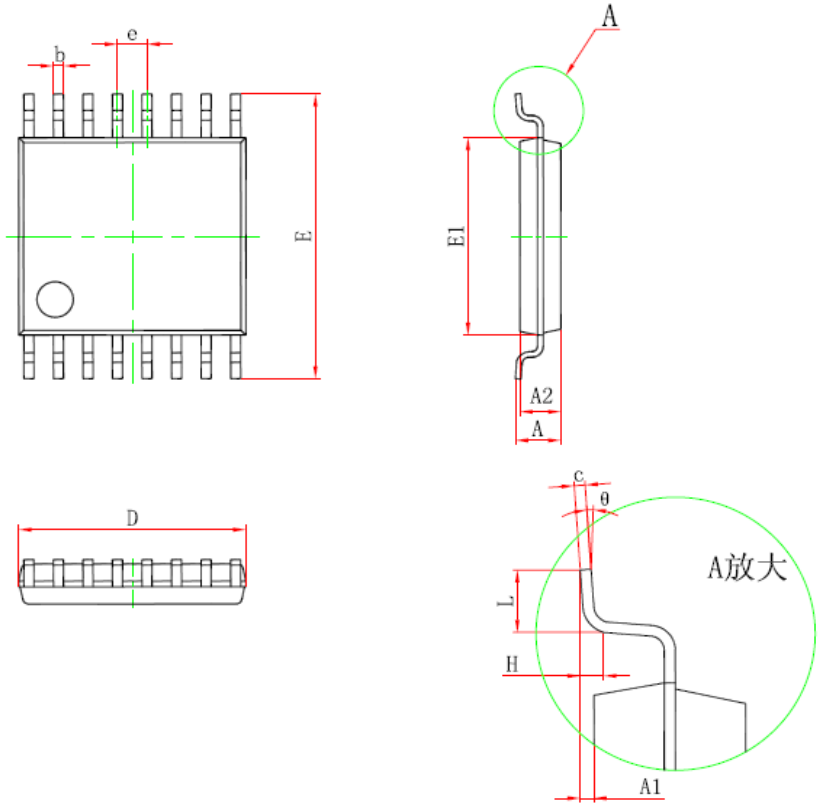
PACKAGE OUTLINE DIMENSIONS

SOP16



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

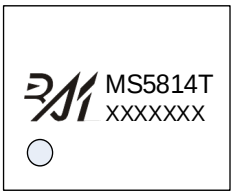
TSSOP16



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
E	6.250	6.550	0.246	0.258
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	4.300	4.500	0.169	0.177
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.400	1.270	0.016	0.050
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name: MS5814, MS5814T

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS5814	SOP16	2500	1	2500	8	20000
MS5814T	TSSOP16	3000	1	3000	8	24000

STATEMENT

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  Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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