Multipoint, Low Voltage Differential Signaling (M-LVDS) Line Driver and Receiver

PRODUCT DESCRIPTION

The MS2111 is a multipoint low voltage differential signaling (M-LVDS) line driver and receiver. It can be optimized to operate at 200 Mbps signal rate and all parts meet the M-LVDS standard TIA/EIA-899. The driver has been designed to support the multipoint buses with load as low as 30Ω.

The receiver of the MS2111 belongs to Type-2, which can detect the bus status with differential input voltage as low as 50mV in the common-mode voltage range of -1V to 3.4V. Type-2 receiver has an offset threshold, which can provide known output status in case of open circuit, idle bus and other faults.

SOP8

FEATURES

- Low Voltage Differential 30Ω to 55Ω Line Driver and Receiver, Signal Rate up to 200Mbps
- Single Power Supply: 3.3V
- Type-2 Receiver Providing Offset Threshold (100mV) to Detect Meeting or Exceeding the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange,
- -1V to 3.4V Common-mode Voltage Range Allowing Data Transmission with 2V Grounding Noise
- When Disabled or VCC≤1.5V, Bus Pin High Impedance
- M-LVDS Bus Power up/down Glitch Free

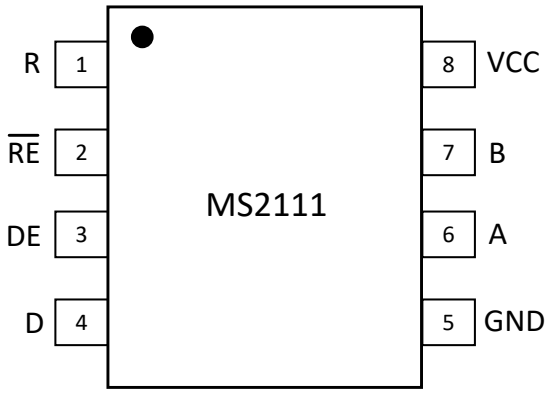
APPLICATIONS

- Low Power Dissipation, High-speed and Short-distance Alternative to TIA/EIA-485
- Backplane or Cabled Multipoint Data and Clock Transmission
- Printer Cellular Base Station
- Central-Office Switch
- Network Switch and Router

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS2111	SOP8	MS2111

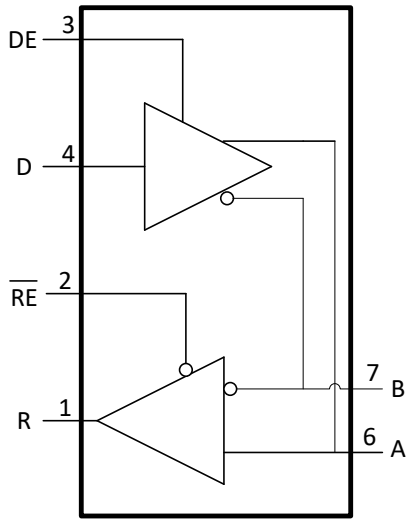
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	R	O	Receiver Output, CMOS Level
2	$\overline{RE}$	I	Receiver Enable, Active Low, CMOS Level
3	DE	I	Driver Enable, Active High, CMOS Level
4	D	I	Driver Data Input, CMOS Level
5	GND	-	Reference Ground
6	A	I/O	Receiver Differential Output/Driver Differential Input
7	B	I/O	Receiver Differential Output/Driver Differential Input
8	VCC	-	Power Supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Condition	Range	Unit
Power Supply	V_{CC}		-0.5 ~ 4	V
Input Voltage		D, DE, $\overline{RE}$	-0.5 ~ 4	V
		A, B	-1.8 ~ 4	V
Output Voltage		R	-0.3 ~ 4	V
		A, B	-1.8 ~ 4	V
Junction Temperature	T_J		-55 ~ 150	°C
Storage Temperature	T_{STG}		-65 ~ 150	°C
Lead Temperature (Unleaded)	T_{PEAK}		260	°C
Duration Time at T_{PEAK} (Unleaded)	T_P		10	s

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC}	3	3.3	3.6	V
High-level Input Voltage	V_{IH}	2		V_{CC}	V
Low-level Input Voltage	V_{IL}	0		0.8	V
Common-mode Input Voltage for A and B Pins	V_{ICM}	-1.4		3.8	V
Differential Input Voltage for A and B Pins	$\|V_{ID}\|$			V_{CC}	V
Differential Load Resistance for A and B Pins	R_L	30	50		Ω
Signal Rate	$1/t_{UI}$			200	Mbps
Operating Temperature	T_A	-40		85	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all power supplies are 3V±10%, T_A=25°C.

Current Parameters

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Driver Current	I_{CCD}	$\overline{RE}$ =DE=V_{CC}, R_L=50Ω, Others Open	16.5	16.7	17	mA
Driver and Receiver Disable Current	I_{CCOFF}	$\overline{RE}$ =V_{CC}, DE=0, Others Open		1.9		mA
Driver and Receiver Enable Current	I_{CCT}	$\overline{RE}$ =0, DE=V_{CC}, R_L=50Ω, Others Open	18.7	19.2	20	mA
Receiver Current	I_{CCR}	$\overline{RE}$ =DE=0, R_L=50Ω, Others Open	4.3	4.5	4.6	mA

Driver Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Differential Output Voltage Magnitude	V_{AB}	See Figure 2	625	640	650	mV
Differential Output Voltage Magnitude Variation	ΔV_{AB}	See Figure 2			20	mV
Common-mode Output Voltage in Steady-state	$V_{OS(SS)}$	See Figure 3	0.99	1.03	1.16	V
Common-mode Output Voltage Variation in Steady-state	$\Delta V_{OS(SS)}$	See Figure 3			50	mV
Peak-to-peak Common-mode Output Voltage in Steady-state	$\Delta V_{OS(PP)}$	See Figure 3			210	mV
Maximum Open-circuit Output Voltage in Steady-state	V_{AOC}	See Figure 7	0.1		1.8	V
Maximum Open-circuit Output Voltage in Steady-state	V_{BOC}	See Figure 7	0.1		1.8	V
Overshoot Output Voltage, Low-to-High Level Output	$V_{P(H)}$	See Figure 5	1.03×V_{SS}		1.1×V_{SS}	V
Overshoot Output Voltage, High-to-Low Level Output	$V_{P(L)}$	See Figure 5	-0.06×V_{SS}		-0.09×V_{SS}	V
High-level Input Current	I_{IH}	V_{IH}=2V		1		μA
Low-level Input Current	I_{IL}	V_{IH}=0.8V		1		μA
Differential Short-circuit Output Current Magnitude	I_{OS}	See Figure 4	12.5	16	19	mA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-impedance Output Current	I_{OZ}	$V_Y \geq -1.4$ or $V_Z \leq 3.8V$, Other Outputs=1.2V		0		μA
Disable Current	$I_{O(OFF)}$	$V_Y \geq -1.4$ or $V_Z \leq 3.8V$, Other Outputs=1.2V, $0 \leq V_{CC} \leq 1.5V$		6		μA
Output Capacitance	C_A or C_B	V_I=0.4× sin(30E6 π t) +0.5V, Other Outputs=1.2V, Driver is disabled			3	pF
Differential Output Capacitance	C_{AB}	V_I=0.4× sin(30E6 π t) +0.5V, Driver is disabled			2.5	pF
Output Capacitance Balance	$C_{A/B}$	C_A/C_B	0.99		1.01	

Driver Switching Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Propagation Delay Time, Low-to-High Output	t_{PLH}	See Figure 5		3.3		ns
Propagation Delay time, High-to-Low Output	t_{PHL}	See Figure 5		3.3		ns
Differential Output Rising Time	t_R	See Figure 5		1.6		ns
Differential Output Falling Time	t_F	See Figure 5		1.6		ns
Propagation Delay Skew($\lvert t_{PHL}-t_{PLH} \rvert$)	$t_{SK(P)}$	See Figure 5		0		ps
Part-to-Part Propagation Delay Skew	$t_{SK(PP)}$	See Figure 5		30		ps
Periodic Jitter, RMS	$t_{JIT(PER)}$	50MHz Clock Input, See Figure 8		7		ps
Cycle-to-cycle Jitter, RMS	$t_{JIT(CC)}$	50MHz clock Input, See Figure 8		5		ps
Peak-to-Peak Jitter	$t_{JIT(PP)}$	100Mbps,2^{15}-1 PRBS Input, See Figure 8		55		ps
Disable time, High-level to High-impedance Output	t_{PHZ}	See Figure 6		5.6		ns
Disable time, Low-level to High-impedance Output	t_{PLZ}	See Figure 6		5.6		ns
Enable time, High-impedance to High-level Output	t_{PZH}	See Figure 6		5.6		ns
Enable time, High-impedance to Low-level Output	t_{PZL}	See Figure 6		5.6		ns

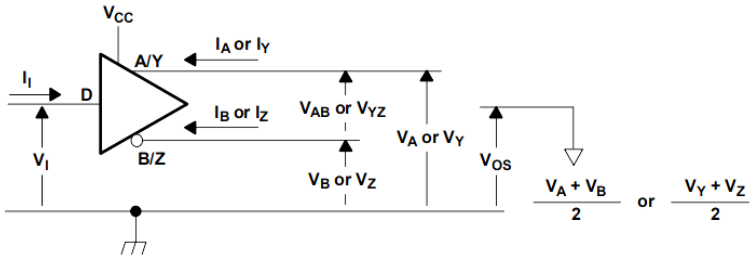


Figure 1. Driver Voltage and Current Definitions

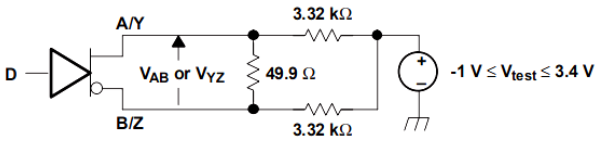


Figure 2. Differential Output Voltage Test Circuit

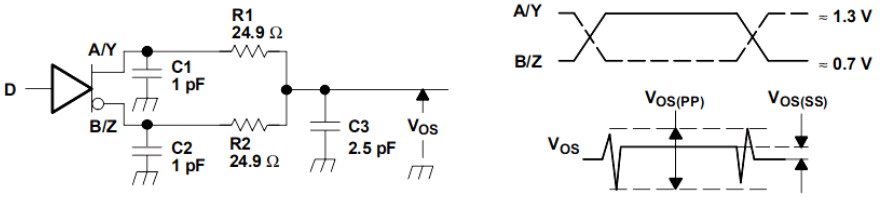


Figure 3. Test Definitions of the Driver Common-mode Output Voltage

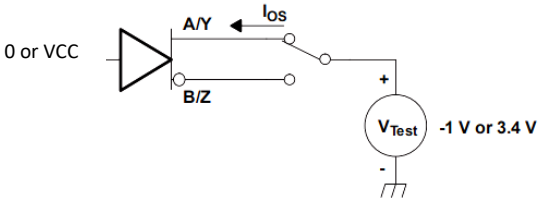


Figure 4. Test Circuit for Output Short-circuit Current

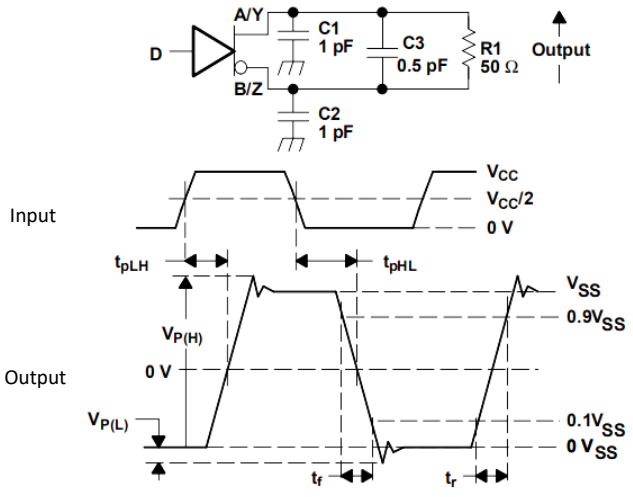


Figure 5. Driver Test Circuit, Timing and Voltage Definitions of Differential Output Signal

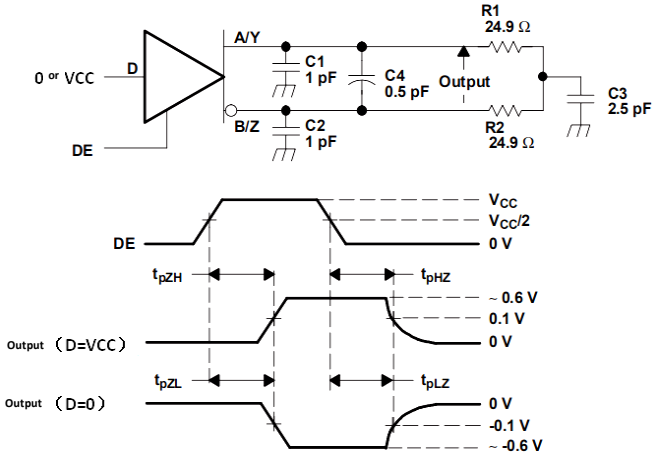


Figure 6. Driver Enable and Disable Time Test Circuit and Definitions

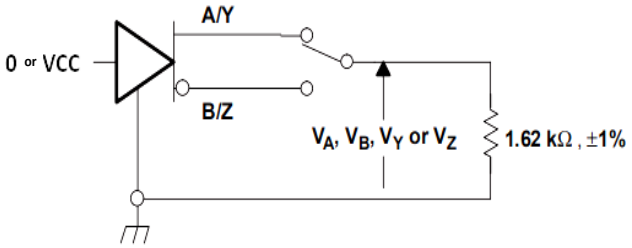


Figure 7. Maximum Output Voltage in Steady-state

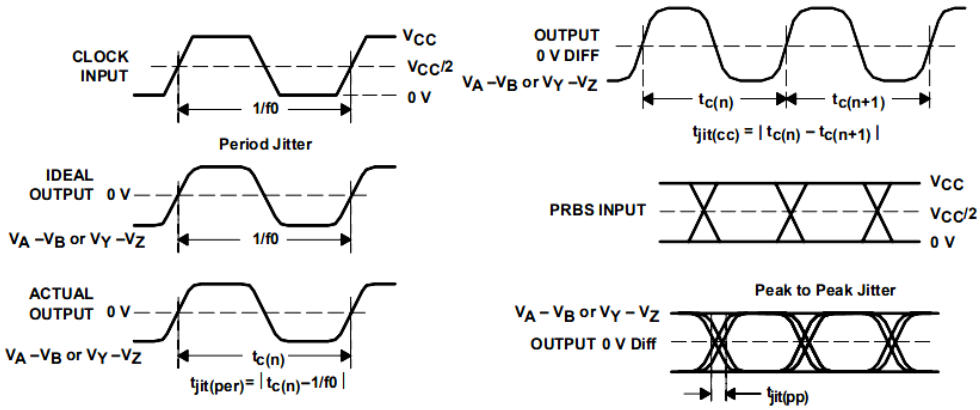


Figure 8. Driver Jitter Measurement Definition

Note:

1. All input pulses have following characteristics: the rising time t_R and the falling time t_F are all less than or equal to 1ns, the frequency=500kHz and the duty cycle is between 45% and 55%.

2. Capacitors like C1, C2, C3 and C4 include the total capacitance of measurement instrumentation and wiring, and are placed within 2cm of the device to be tested.

3.R1 and R2 are surface mounted resistors, 1% error and placed within 2cm of the device to be tested.

4.The measurement of $V_{OS(PP)}$ requires the test equipment with a -3dB bandwidth of at least 1GHz.

Receiver Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Positive-going Differential Input Voltage Threshold	V_{IT+}	See Figure 9, Table 1	136	170	213	mV
Negative-going Differential Input Voltage Threshold	V_{IT-}	See Figure 9, Table 1	13	50	77	mV
High-level Output Voltage	V_{OH}	I_{OH}=-8mA	2.81	3.0	3.07	V
Low-level Output Voltage	V_{OL}	I_{OL}=8mA	0.1	0.21	0.34	V
High-level Input Current	I_{IH}	V_{IH}=2V	-3	-2	-1	μA
Low-level Input Current	I_{IL}	V_{IL}=0.8V	-4	-1	0	μA
High-impedance Output Current	I_{OZ}	V_O=0 or 3.6V	0		1	μA
Input Capacitance	C_A or C_B	V_I=0.4×sin(30E6 π t)+0.5V, Other inputs=1.2V, Driver is disabled			3	pF
Differential Input Capacitance	C_{AB}	V_I=0.4×sin(30E6 π t)+0.5V, Driver is disabled			2.5	pF
Input Capacitance Balance	$C_{A/B}$	C_A/C_B	0.99		1.01	

Receiver Switching Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Propagation Delay Time, Low-to-High Output	t_{PLH}	C_L=15pF, See Figure 10	6	7.2		ns
Propagation Delay Time, High-to-Low Output	t_{PHL}	C_L=15pF, See Figure 10	6	7.2		ns
Differential Output Rising Time	t_R	C_L=15pF, See Figure 10	3.2	3.6		ns
Differential Output Falling Time	t_F	C_L=15pF, See Figure 10	3.2	3.6		ns
Propagation Delay Skew($\lvert t_{PHL}-t_{PLH} \rvert$)	$t_{SK(P)}$	C_L=15pF, See Figure 10	3.2	100		ps
Part-to-Part Delay Skew	$t_{SK(PP)}$	C_L=15pF, See Figure 10		300		ps
Disable time, High-level to High-impedance Output	t_{PHZ}	See Figure 11	7	9.2		ns
Disable time, Low-level to High-impedance Output	t_{PLZ}	See Figure 11	7	9.2		ns
Enable Time, High-impedance to High-level Output	t_{PZH}	See Figure 11	12	14		ns

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Enable time, High-impedance to Low-level Output	t_{PZL}	See Figure 11	12	14		ns
Periodic Jitter, RMS	$t_{JIT(PER)}$	50MHz Clock Input, See Figure 12		10		ps
Cycle-to-Cycle Jitter, Peak Value	$t_{JIT(CC)}$	50MHz Clock Input, See Figure 12		400		ps
Peak-to-Peak Jitter	$t_{JIT(PP)}$	100Mbps,2^{15}-1 PRBS Input, See Figure 12		560		ps

Notes about the Above Table:

The measurement of receiver jitter: input voltage V_{ID}=400mVpp, input common-mode voltage V_{CM}=1V. Periodic jitter and cycle-to-cycle jitter measure 30000 data. And peak-to-peak jitter measures 100000 data.

Table 1. Receiver Input Threshold Test Voltages

Input Voltage		Differential Input Voltage	Common-mode Input Voltage	Receiver Output
V_A	V_B	V_{ID}	V_{CM}	R
2.4	0	2.4	1.2	H
0	2.4	-2.4	1.2	L
3.8	3.65	0.15	3.725	H
3.8	3.75	0.05	3.775	L
-1.25	-1.4	0.15	-1.325	H
-1.35	-1.4	0.05	-1.375	L

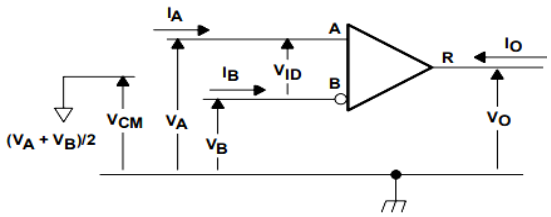
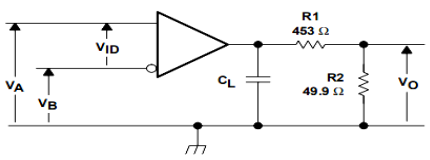


Figure 9. Receiver Voltage and Current Definitions



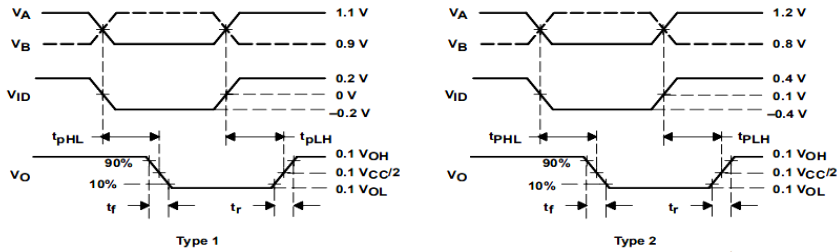


Figure 10. Receiver Timing Test Definition

Notes about the Figure 10:

1. All input pulses have following characteristics: rising time t_R and falling time t_F are less than or equal to 1ns, frequency is 500kHz and duty cycle is between 45% ~ 55%.
2. R1 is a metal film SMD resistor, 1% error and placed within 2cm of the device to be tested.
3. C_L is a non-loss ceramic chip capacitor with 20% error and placed within 2cm of the device to be tested.
4. R2 is placed within 15cm of the device to be tested.

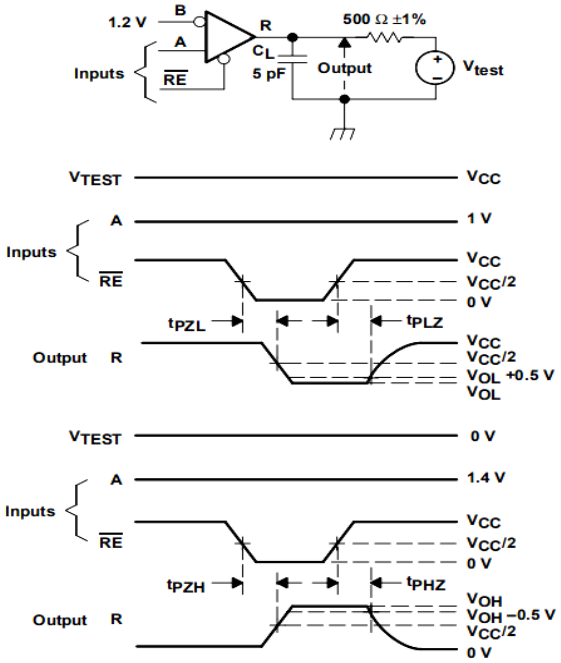


Figure 11. Receiver Enable/Disable Time Test Definition

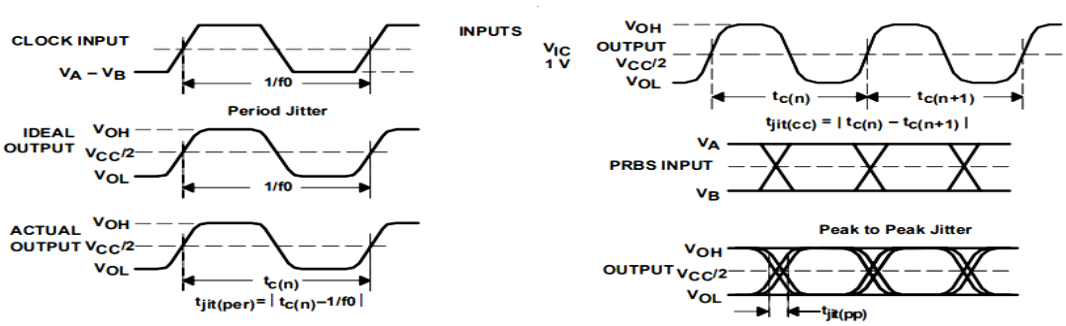
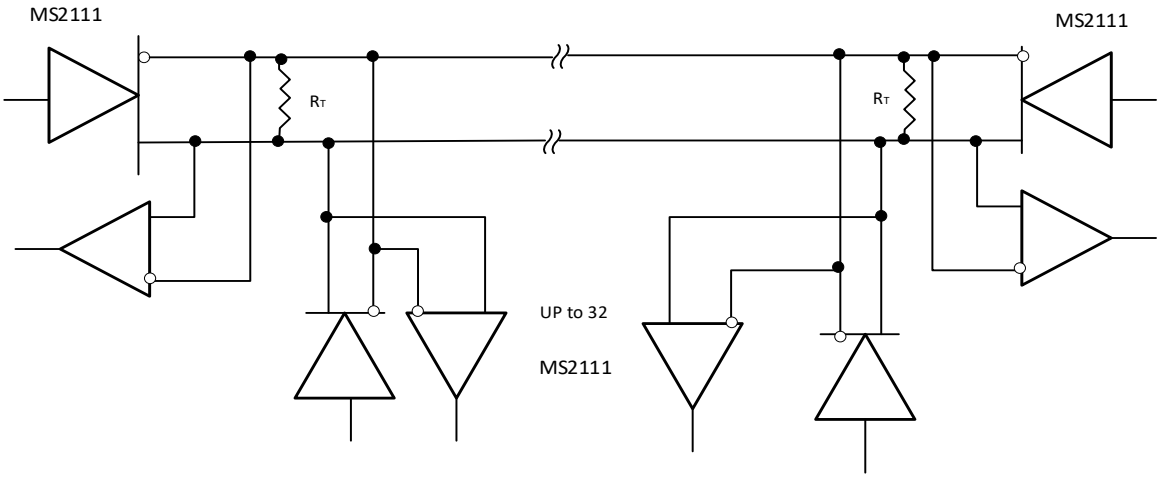


Figure 12. Receiver Jitter Measurement Definition

Bus Input and Output Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Receiver Input Current or Transceiver Input/Output Current with Driver Disabled	I_A	V_A=3.8V, V_B=1.2V	4.7	5.5	8	μA
		V_A=0 or 2.4V, V_B=1.2V	-15	-10.5	-8	μA
		V_A=-1.4V, V_B=1.2V	-21	-15.4	-12	μA
Receiver Input Current or Transceiver Input/Output Current with Driver Disabled	I_B	V_B=3.8V, V_A=1.2V	4.7	5.5	8	μA
		V_B=0 or 2.4V, V_A=1.2V	-15	-10.5	-8	μA
		V_B=-1.4V, V_A=1.2V	-21	-15.4	-12	μA
Receiver Differential Input Current or Transceiver Differential Input/Output Current(I_A-I_B) with Driver Disabled	I_{AB}	V_B=V_A, -1.4V ≤V_A≤3.8V		0		μA
Receiver or Transceiver Power-off Input Current	$I_{A(OFF)}$	V_A=3.8V, V_B=1.2V 0V ≤V_{CC}≤1.5V	12	14	17	μA
		V_A=0 or 2.4V, V_B=1.2V, 0V ≤V_{CC}≤1.5V	-7	-3	8	μA
		V_B=-1.4V, V_A=1.2V, 0V ≤V_{CC}≤1.5V	-11	-6	-5	μA
Receiver or Transceiver Power-off Input Current	$I_{B(OFF)}$	V_B=3.8V, V_A=1.2V 0V ≤V_{CC}≤1.5V	12	14	17	μA
		V_B=0 or 2.4V, V_A=1.2V, 0V ≤V_{CC}≤1.5V	-7	-3	8	μA
		V_B=-1.4V, V_A=1.2V, 0V ≤V_{CC}≤1.5V	-11	-6	-5	μA
Receiver or Transceiver Power-off Differential Input Current	$I_{AB(OFF)}$	V_B=V_A,-1.4V ≤V_A≤3.8V 0V ≤V_{CC}≤1.5V		0		μA
Transceiver Input Capacitance with Driver Disabled	C_A	V_A=0.4×sin(30E6 π t)+0.5V, V_B=1.2V			3	pF
Transceiver Input Capacitance with Driver Disabled	C_B	V_B=0.4×sin(30E6 π t)+0.5V, V_A=1.2V			3	pF
Transceiver Differential Input Capacitance with Driver Disabled	C_{AB}	V_{AB}=0.4× sin(30E6 π t)+0.5V			2.5	pF
Output Capacitance Balance with Driver Disabled	$C_{A/B}$	C_A/C_B	0.99		1.01	

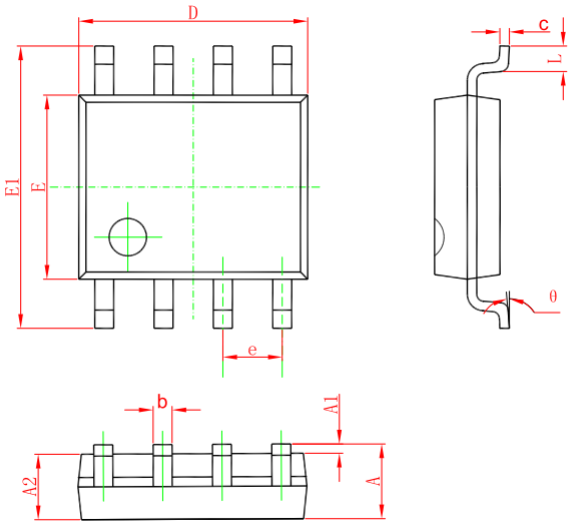
TYPICAL APPLICATION DIAGRAM



Note: As shown in the figure above, R_T=100Ω, and it must be placed at both sides.

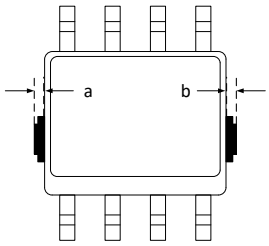
PACKAGE OUTLINE DIMENSIONS

SOP8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27BSC		0.050BSC	
L	0.400	1.270	0.016	0.050
θ	0 º	8 º	0 º	8 º

Note: In addition to the package size, a, b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.



MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description

Product Name: MS2111

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS2111	SOP8	4000	1	4000	8	32000

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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