# Quad DMOS Full Bridge Driver

PRODUCT DESCRIPTION

The MS35632N/MS35632P is a quad DMOS full bridge driver, which can drive two stepper motors or four DC motors. The driving current of each full bridge can be up to 1.2A at 24V. The MS35632N/MS35632P integrates a fixed off-time PWM current regulator and a 2bit nonlinear DAC, and could operate in full, half, quarter steps and forward, reverse, standby modes. PWM current regulator uses mixed decay mode, which can reduce audio motor noise and power dissipation and improve step accuracy. The chip integrates internal synchronous rectification control circuit to reduce PWM operating power dissipation.

The chip integrates protection circuits, such as undervoltage protection (UVLO), overturning current protection and thermal shutdown. Therefore, the specified power starting sequence is not required.
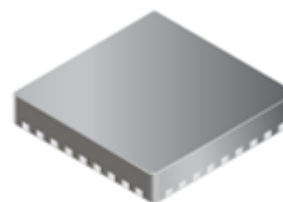
QFN36

TQFP48

FEATURES

- Quad Full Bridge
- Dual Stepper Motor Driving
- Large Current Output
- 3.3V and 5V Logics
- Synchronous Rectification
- Built-in UVLO
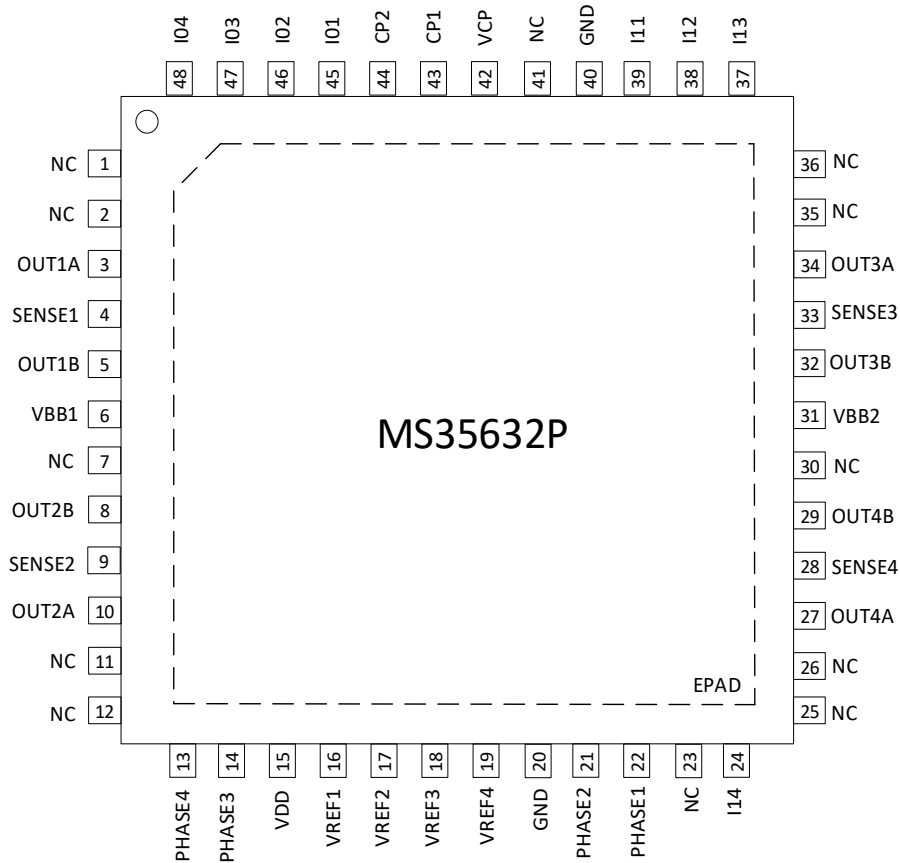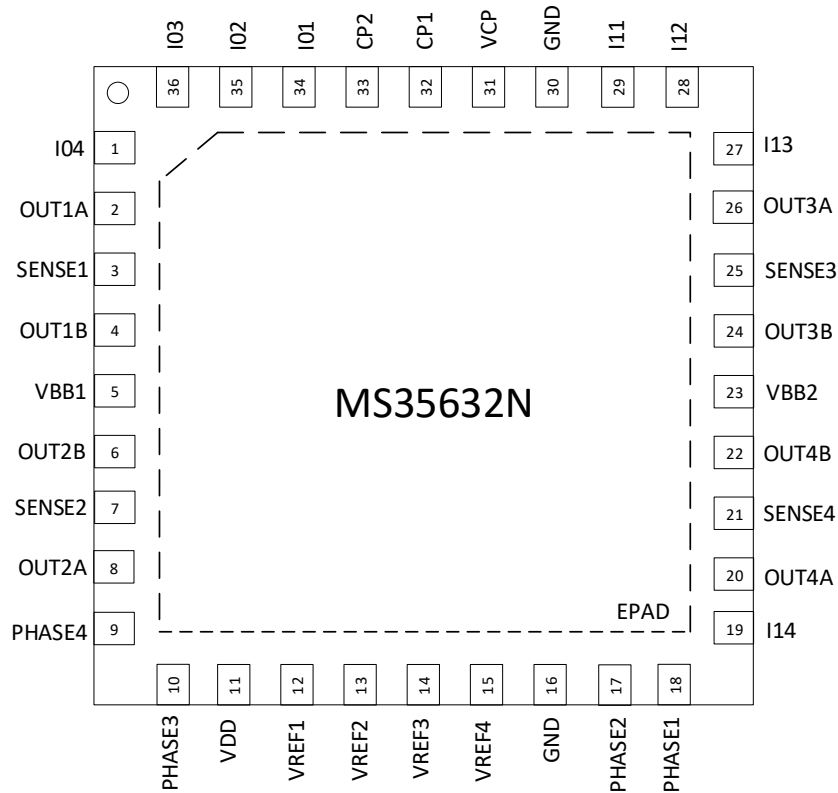- Overturn Protection
- Thermal Shutdown

APPLICATIONS

- Security Monitoring
- Stage Lights
- Toys
- Robotic Technology
- Medical Equipment

PRODUCT SPECIFICATIONS

Part Number	Package	Marking
MS35632N	QFN36	MS35632N
*MS35632P	TQFP48	MS35632P

*The package is not available temporarily. If necessary, please contact Hangzhou Ruimeng Sales Department Center.

PIN CONFIGURATION

MS35632N

Top pins (36–28): IO3, IO2, IO1, CP2, CP1, VCP, GND, I11, I12

Left pins (1–9): IO4, OUT1A, SENSE1, OUT1B, VBB1, OUT2B, SENSE2, OUT2A, PHASE4

Right pins (27–19): I13, OUT3A, SENSE3, OUT3B, VBB2, OUT4B, SENSE4, OUT4A, I14

Bottom pins (10–18): PHASE3, VDD, VREF1, VREF2, VREF3, VREF4, GND, PHASE2, PHASE1

EPAD

MS35632P

Top pins (48–37): IO4, IO3, IO2, IO1, CP2, CP1, VCP, NC, GND, I11, I12, I13

Left pins (1–12): NC, NC, OUT1A, SENSE1, OUT1B, VBB1, NC, OUT2B, SENSE2, OUT2A, NC, NC

Right pins (36–25): NC, NC, OUT3A, SENSE3, OUT3B, VBB2, NC, OUT4B, SENSE4, OUT4A, NC, NC

Bottom pins (13–24): PHASE4, PHASE3, VDD, VREF1, VREF2, VREF3, VREF4, GND, PHASE2, PHASE1, NC, I14

EPAD

PIN DESCRIPTION

Pin		Name	Description
MS35632N	MS35632P		
2	3	OUT1A	DMOS H-Bridge Channel 1 Output A
3	4	SENSE1	Channel 1, SENSE Resistor Pin
4	5	OUT1B	DMOS H-Bridge Channel 1 Output B
5	6	VBB1	Power Supply
6	8	OUT2B	DMOS H-Bridge Channel 2 Output B
7	9	SENSE2	Channel 2, SENSE Resistor Pin
8	10	OUT2A	DMOS H-Bridge Channel 2 Output A
9	13	PHASE4	Channel 4, Control Input Pin
10	14	PHASE3	Channel 3, Control Input Pin
11	15	VDD	Logic Power Supply
12	16	VREF1	Channel 1, Analog Input Pin
13	17	VREF2	Channel 2, Analog Input Pin
14	18	VREF3	Channel 3, Analog Input Pin
15	19	VREF4	Channel 4, Analog Input Pin
16	20	GND	Ground
17	21	PHASE2	Channel 2, Control Input Pin
18	22	PHASE1	Channel 1, Control Input Pin
19	24	I14	Channel 4, Control Input Pin
20	27	OUT4A	DMOS H-Bridge Channel 4 Output A
21	28	SENSE4	Channel 4, SENSE Resistor Pin
22	29	OUT4B	DMOS H-Bridge Channel 4 Output B
23	31	VBB2	Power Supply
24	32	OUT3B	DMOS H-Bridge Channel 3 Output B
25	33	SENSE3	Channel 3, SENSE Resistor Pin
26	34	OUT3A	DMOS H-Bridge Channel 3 Output A
27	37	I13	Channel 3, Control Input Pin
28	38	I12	Channel 2, Control Input Pin
29	39	I11	Channel 1, Control Input Pin
30	40	GND	Ground

Pin		Name	Description
MS35632N	MS35632P		
31	42	VCP	Reservoir Charge Capacitor Pin
32	43	CP1	Charge-pump Capacitor Pin
33	44	CP2	Charge-pump Capacitor Pin
34	45	I01	Channel 1, Control Input Pin
35	46	I02	Channel 2, Control Input Pin
36	47	I03	Channel 3, Control Input Pin
1	48	I04	Channel 4, Control Input Pin
-	1,2,7,11,12,23, 25,26,30,35, 36,41	NC	Not Connection
-	-	EPAD	Exposed Thermal Pad, Soldered to PCB directly and connected to ground

BLOCK DIAGRAM
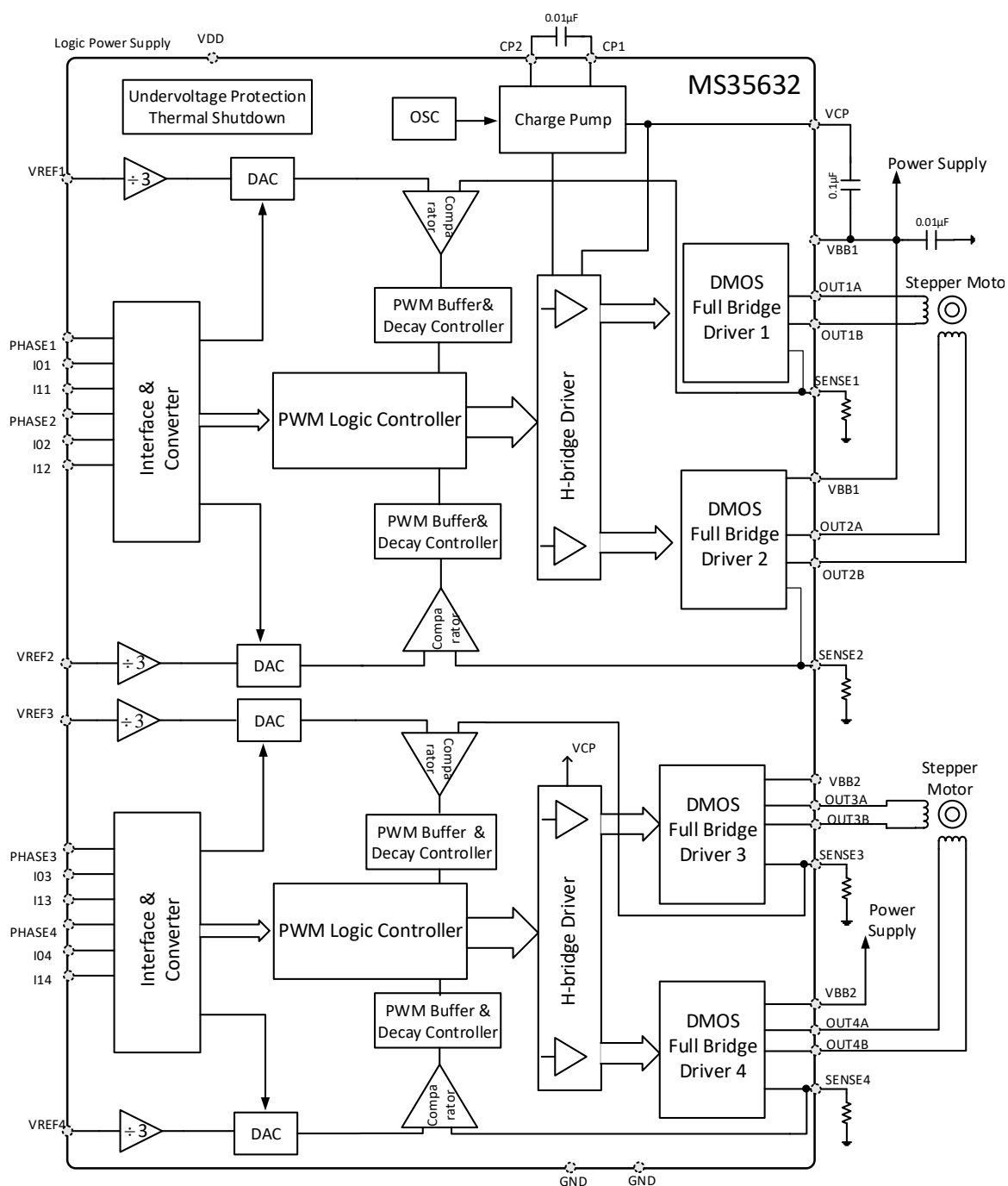
ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	V_{BB}	-0.5 ~ 38	V
Logic Power Supply	V_{DD}	-0.4 ~ 6	V
Output Current	I_{OUT}	1.2	A
Logic Input Voltage	V_{IN}	-0.3 ~ 6	V
Voltage on SENSEx Pin	V_{SENSEx}	0.5	V
Voltage on VREFx Pin	V_{REFX}	2.5	V
Operating Temperature	T_A	-40 ~ 105	°C
Junction Temperature	T_{JMAX}	150	°C
Storage Temperature	T_{STG}	-65 ~ 150	°C
ESD(HBM)	V_{ESD}	>±3k	V

Thermal Resistance

Parameter	Symbol	MS35632N QFN36	MS35632P TQFP48	Unit
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	19.02	17.50	°C/W

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A= 25°C ±2°C, V_{BB}=24V, V_{DD}=3.3V.

Power Supply

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply	V_{BB}		8		36	V
Logic Power Supply	V_{DD}		3		5.5	V
Power Supply Current	I_{BB}			2.4	10	mA
Logic Supply Current	I_{DD}			1.84		mA

Output Power Transistor

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-side Transistor Output On-Resistance	R_{DSONH}	I_{OUT}=500mA,T_J=25°C		0.5	0.7	Ω
Low-side Transistor Output On-Resistance	R_{DSONL}	I_{OUT}=500mA,T_J=25°C		0.5	0.8	Ω

Logic and Low Voltage Input

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input Voltage	$V_{IN(H)}$		0.7×V_{DD}		V_{DD}+0.3	V
Low-level Input Voltage	$V_{IN(L)}$		-0.3		0.3×V_{DD}	V
VREFx Input Voltage	V_{REFX}		0		2.5	V
VREFx Input Current	I_{REF}	V_{REF}=1.5V			±1	μA

Timing

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Propagation Delay	t_{D1}	PWM Conversion, HS Transistor Open	350	550	1000	ns
	t_{D2}	PWM Conversion, HS Transistor Closed	35		300	ns
	t_{D3}	PWM Conversion, LS Transistor Open	350	550	1000	ns
	t_{D4}	PWM Conversion, LS Transistor Closed	35		250	ns
Overturn Delay	t_{COD}		300	425	1000	ns
Blank Time	t_{BLANK}		0.7	1	1.3	μs

Output Current Accuracy

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Current Error[1]	V_{ERR}	V_{REF}=1.5V, Phase Current 100%	-5		5	%
		V_{REF}=1.5V, Phase Current 67%	-5		5	%
		V_{REF}=1.5V, Phase Current 33%	-15		15	%

Note 1: $V_{ERR} = (V_{REF}/3 - V_{SENSE})/(V_{REF}/3)$.

Protection Circuit

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VBB Undervoltage Protection	$V_{UV(VBB)}$	V_{BB} Rising	6.5	6.8	7.1	V
VBB Undervoltage Hysteresis	$V_{UV(VBB)HYS}$		0.3	0.4	0.5	V
VDD Undervoltage Protection	$V_{UV(VDD)}$	V_{DD} Rising	2.6	2.7	2.8	V
VDD Undervoltage Hysteresis	$V_{UV(VDD)HYS}$		75	105	125	mV
Thermal Shutdown	T_{JSD}	Temperature Rising	155	165	175	°C
Thermal Shutdown Hysteresis	T_{JSD_HYS}			15		°C

FUNCTION DESCRIPTION

Device Characteristics

The MS35632N/MS35632P could drive two stepper motors or four DC motors, a stepper motor and two DC motors can also be driven. The output H full bridge is consisted of four N-channel DMOS, controlled by PWM. The output peak current of each full bridge is decided by R_{SENSEx} and V_{REFx}. The input pins include PHASEX, I0x and I1x.

Internal PWM Current Control Principle

Each full bridge has PWM current control circuit with fixed decay time, which makes load current not exceed ITRIP. At the initial stage, one H-bridge diagonal pair of source and drain DMOS are enabled, and current flows through motor and R_{SENSE}. When the voltage on R_{SENSE} is equal to one third of VREF voltage, current detection comparator would reset PWM controller and disable source DMOS. The maximum current limit is determined by R_{SENSE} and the voltage on VREF terminal. The maximum current is calculated:

$$ITripMax=VREF /(3{\times}R_{SENSE})$$

Each stepping current limit, ITrip, is the percentage of maximum current limit ITripMax. ITrip can be calculated by:

$$ITrip =(\% \ ITripMax /100){\times}ITripMax$$

Where, please refer to step sequence table for % ITripMax. Note that the maximum voltage on R_{SENSE} doesn't exceed ±500mV in application.

Fixed Off-time

Internal PWM control circuit integrates one fixed-time pulse to disable drivers, the OFF time t_{OFF} is set to 10μs.

Blank Time

When internal circuit control makes output change, the output of current detection comparator would be ignored within blank time to avoid output false detection, for example, reverse recovery current of clamp diode or instantaneous switching of load capacitor causes overcurrent. The blank time is set to 1μs.

Control Logic

The communication between device and controller is transmitted via industry standard I1, I0 and PHASE interface. Full, half, quarter step modes can be realized by control logic. Each H bridge sets independent VREF pin and more precise step modes can be achieved by dynamically controlling VREF pin.

Charge-pump (CP1, CP2)

The charge-pump circuit generates a higher power supply than VBB to drive the source DMOS of H bridge. In application, due to the need for charge and discharge, a 0.1μF ceramic capacitor is needed to be connected between CP1 and CP2. A 0.1μF ceramic capacitor is also required between VCP and VBBx to store charge.

Protection Function

The MS35632N/MS35632P integrates complete protection function, including undervoltage protection and overcurrent protection.

Synchronous Rectification

When the internal fixed decay time circuit is triggered and the PWM-off works, the load current will return. During current decay, the MS35632N/MS35632P synchronous rectification function will enable the corresponding DMOS and short the parasitic diode with Rdson to reduce power consumption effectively. When detecting zero current, synchronous rectification is turned off to prevent the load current from reversing.

Mixed Decay Mode

H bridge operates in mixed decay mode as shown in following figures. When current reaches current limit, fast decay mode is entered and the duration time (t_{FD}) occupies 33% of total decay period. Then system enters slow decay mode. During the conversion from fast to slow decay modes, driver would be disabled for 300ns (dead time). The setting could avoid bridge throughout.
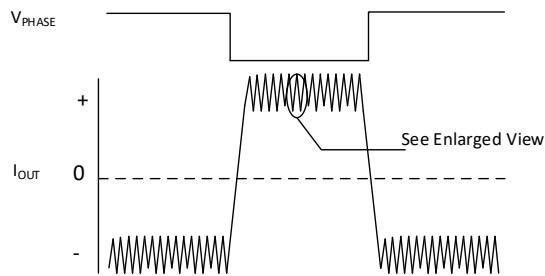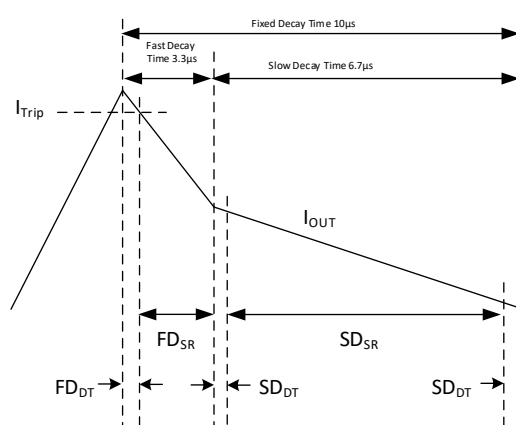
Figure 1. Mixed Decay Mode

Figure 2. Enlarged View of Mixed Decay Mode
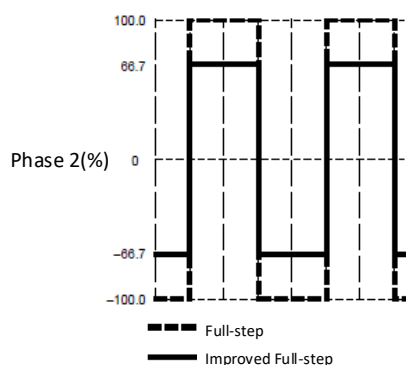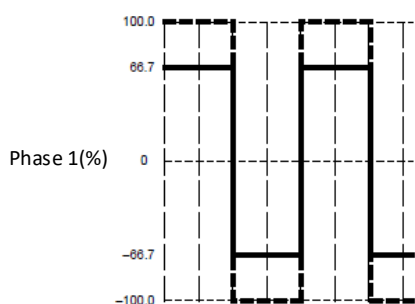
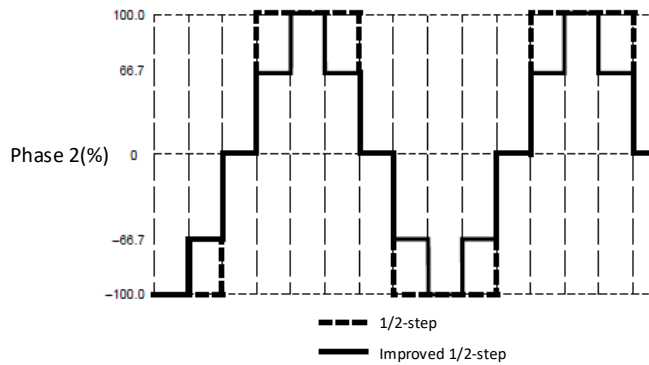**Step Sequencing Diagram**
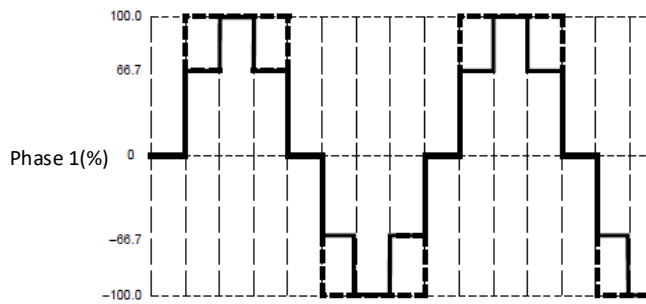

Figure 3. Full-step Phase Sequence Diagram
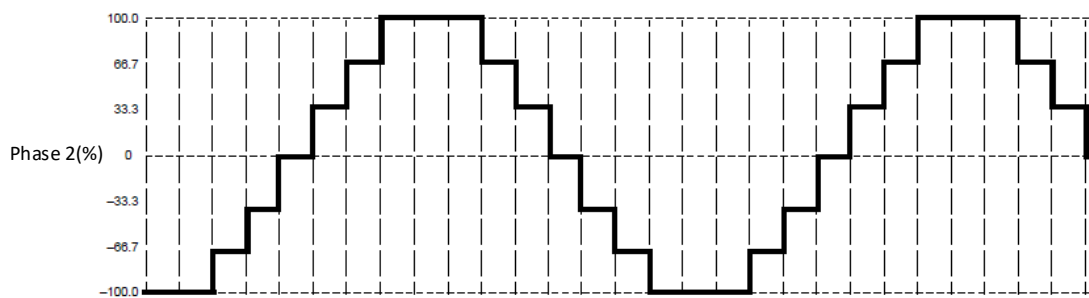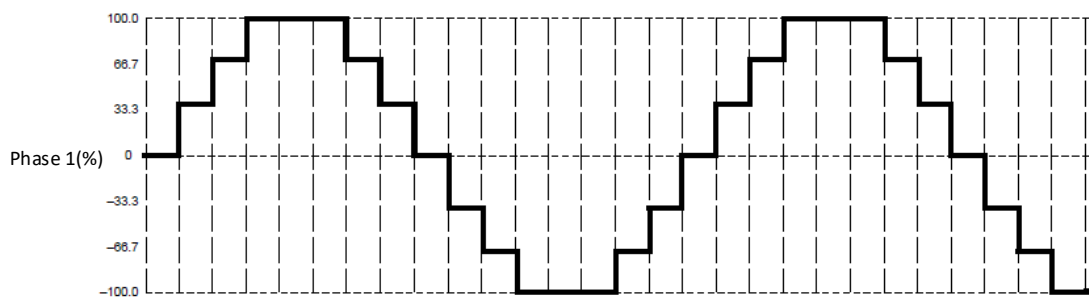

Figure 4. 1/2-step Phase Sequence Diagram

Figure 5. 1/4-step Phase Sequence Diagram

Step Sequencing Setting

Full	1/2	1/4	Phase 1 (% I$_{TripMax}$)	xI0	xI1	Phase	Phase 2 (% I$_{TripMax}$)	xI0	xI1	Phase
	1	1	0	H	H	X	100	L	L	0
		2	33	L	H	1	100	L	L	0
1	2	3	100/66*	L/H*	L	1	100/66*	L/H*	L	0
		4	100	L	L	1	33	L	H	0
	3	5	100	L	L	1	0	H	H	X
		6	100	L	L	1	33	L	H	1
2	4	7	100/66*	L/H*	L	1	100/66*	L/H*	L	1
		8	33	L	H	1	100	L	L	1
	5	9	0	H	H	X	100	L	L	1
		10	33	L	H	0	100	L	L	1
3	6	11	100/66*	L/H*	L	0	100/66*	L/H*	L	1
		12	100	L	L	0	33	L	H	1
	7	13	100	L	L	0	0	H	H	X
		14	100	L	L	0	33	L	H	0
4	8	15	100/66*	L/H*	L	0	100/66*	L/H*	L	0
		16	33	L	H	0	100	L	L	0

*Improved Step Mode

TYPICAL APPLICATION
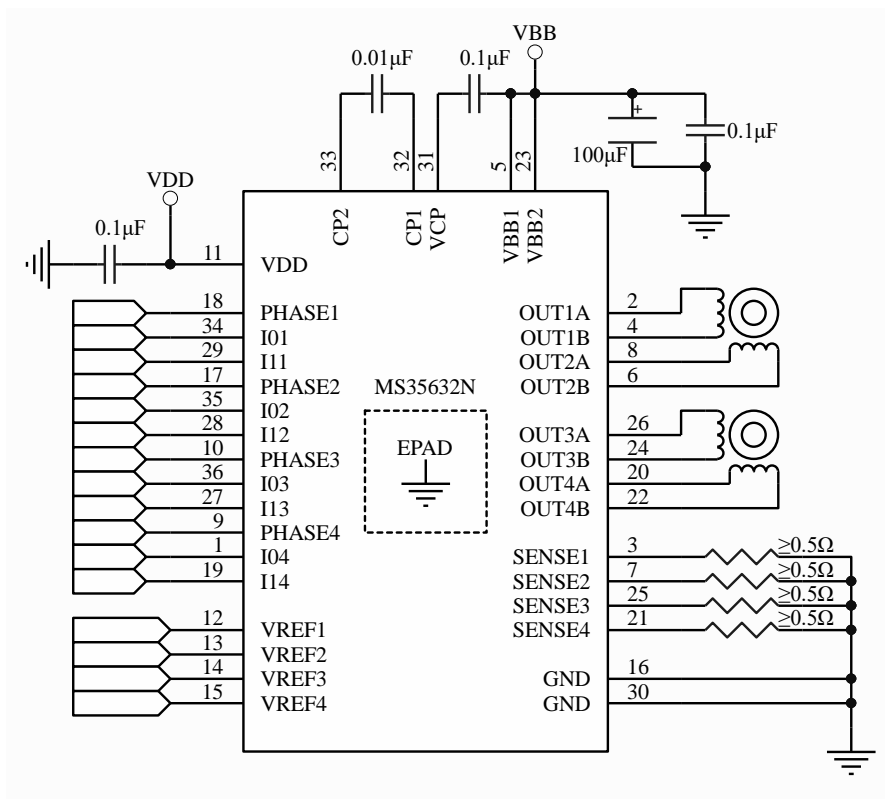

DC Motor Control

The chip integrates four H-bridge drives, each of which is equipped with an independent PWM current control circuit, so it can drive four DC motors. In application, the maximum current can be set by the VREF pin, and the I0x, I1x and PHASEx pins can be controlled by PWM signal to control forward rotation, reverse rotation and standby of the motor.

Layout Making

Heavy ground plane is required for printed circuit board. In order to achieve better performance and heat dissipation, the MS35632N/MS35632P should be directly soldered to the board. On the back of the MS35632N/MS35632P is a metal heat sink, which is directly soldered on the exposed PCB board to radiate heat to other layers.

Layout Ground Trace

In order to reduce ground drift, it is necessary to set one special ground trace with single point and low impedance near the chip in PCB. Generally, the grounding plane directly below the heat sink of the MS35632N/MS35632P is an ideal special ground wire position. Special ground trace with low impedance could effectively avoid ground drift and ensure the stability of power supply.
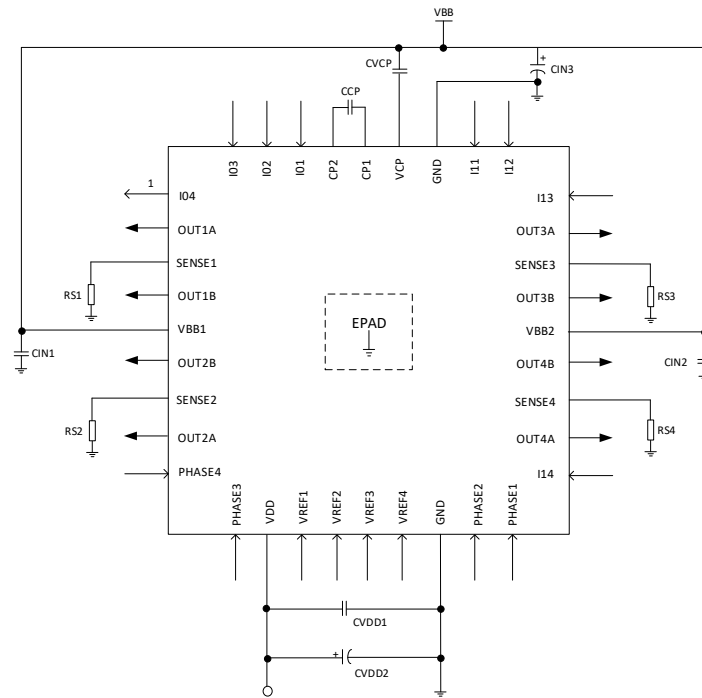
SENSE Pin Setting

R_{SENSEx} resistor on SENSE pin must be connected with one low impedance path to ground. Because the large current flows through R_{SENSEx} and generates accurate feedback voltage to SENSE comparator. Long ground trace would generate extra resistance, thus causing uncertain voltage drop and reducing the accuracy of SENSE comparator. When selecting SENSE resistor, note that the voltage on SENSE pin should not exceed ±500mV in operation.
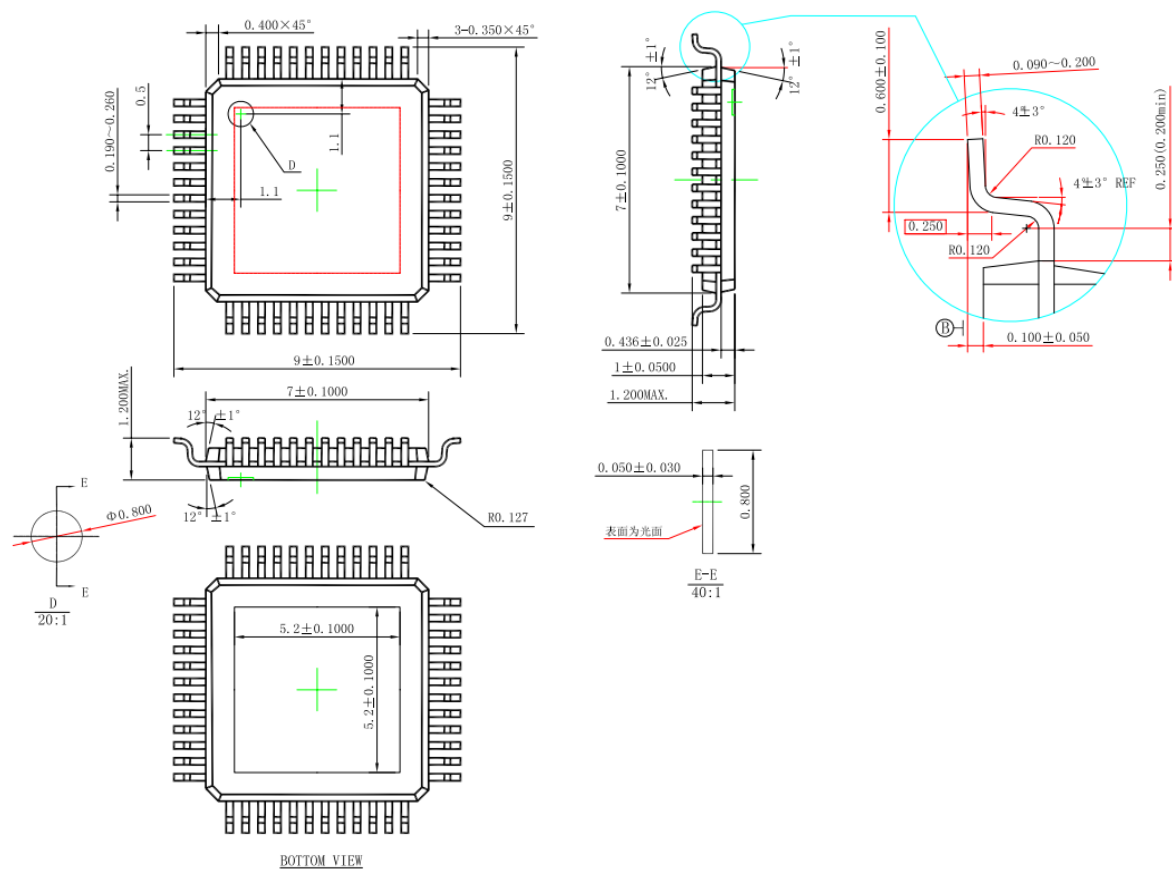
PACKAGE OUTLINE DIMENSIONS

QFN36(06X06) (Back Thermal Pad)
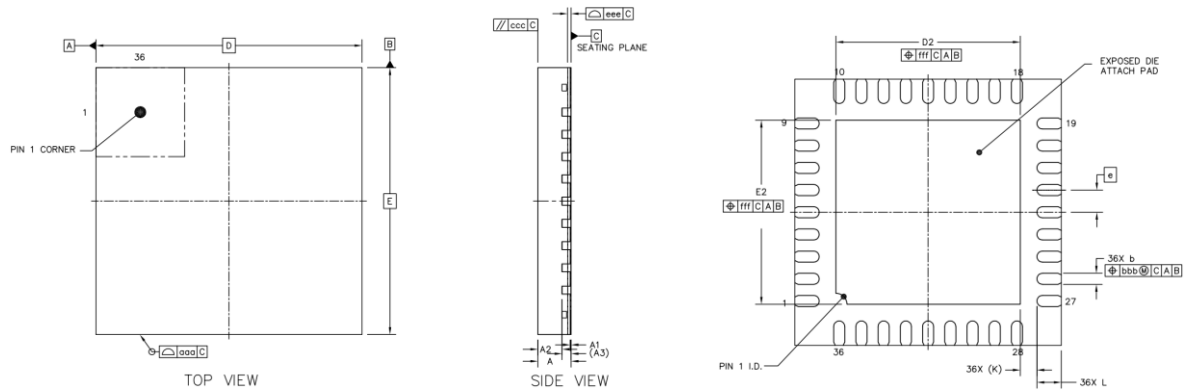
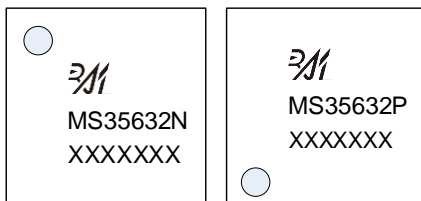| Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.203REF		
b	0.2	0.25	0.3
D	6BSC		
E	6BSC		
e	0.5BSC		
D2	4.05	4.15	4.25
E2	4.05	4.15	4.25
L	0.45	0.55	0.65
K	0.375REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
fff	0.1		

TQFP48(07X07)(Back Thermal Pad)

BOTTOM VIEW

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description

Product Name : MS35632N, MS35632P

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS35632N	QFN36	2000	1	2000	8	16000

Device	Package	Piece/Tray	Tray/Box	Piece/Box	Box/Carton	Piece/Carton
MS35632P	TQFP48	250	10	2500	4	10000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

  Customer should get latest version information and verify the integrity before placing order.

- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety

  standard and adopt corresponding precautions, in order to avoid personal injury and property loss

  caused by potential failure risk.

- The process of improving product is endless. And our company would sincerely provide more excellent

  product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken

to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1、The operator shall ground through the anti-static wristband.

2、The equipment shell must be grounded.

3、The tools used in the assembly process must be grounded.

4、Must use conductor packaging or anti-static materials packaging or transportation.

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