H-bridge Gate Drive Controller

FEATURES

- Single-channel H-bridge Gate Driver

  -Drive Four External N-channel MOSFET

  -Support 100% Pulse Width Modulation (PWM) Duty Cycle

- Operating Power Supply Range: 5.5V to 45V
- Three Control Modes:

  -PH/EN, Independent H-bridge and PWM

- Adjustable Slew Rate Control
- Independent Control of Each H-bridge
- Support 1.8V, 3.3V and 5V Logic Inputs
- Current-shunt Amplifier
- Integrated PWM Current Regulation
- Low Power-Dissipation Sleep Mode
- Protection Characteristics

  -Power Supply Undervoltage Lockout (UVLO)

  -Charge-pump Undervoltage (CPUV) Lockout

  -Overcurrent Protection (OCP)

  -Gate Drive Fault (GDF)

  -Thermal Shutdown (TSD)

  -Fault Regulation Output (nFAULT)

- AEC-Q100 Certification

APPLICATIONS

- Electric Window Regulator, Skylight, Seat, Sliding Door, Trunk and Tailgate
- Relay
- Brushed DC Pumps

PRODUCT DESCRIPTION

The MS31702NA is a small single-channel H-bridge gate driver, which uses four external N-channel MOSFET to drive a bidirectional brushed DC motor.

PH/EN, independent H-bridge or PWM are allowed to be connected to the controller circuit easily. The internal sense amplifier can provide adjustable current control. And the integrated charge pumps can provide 100% duty ratio as well as driving external reverse battery switch.

The independent H-bridge mode supports H-bridge sharing and controls several DC motors. The MS31702NA has the built-in circuit, which uses the PWM current chopping with fixed off-time to adjust winding current.

The MS31702NA can reduce electromagnetic interference (EMI) by the programmable slew rate control technology. It can also be applied flexibly and prevent any gate short-circuit issues.
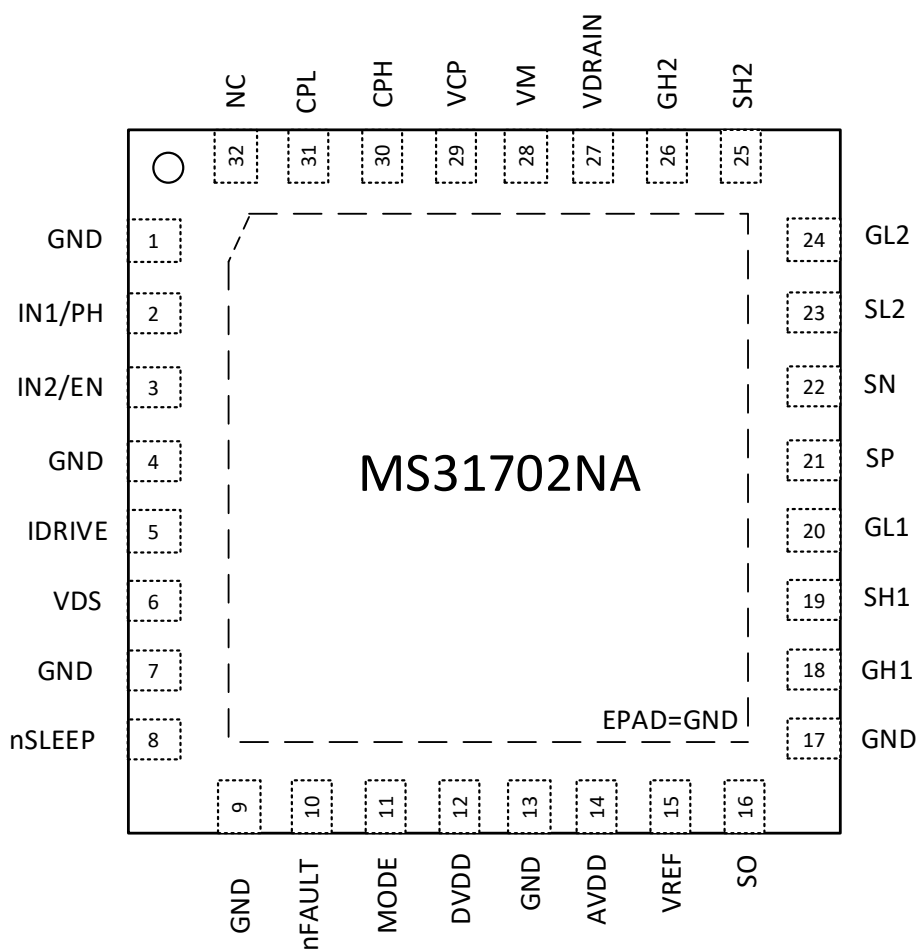
PRODUCT SPECIFICATION

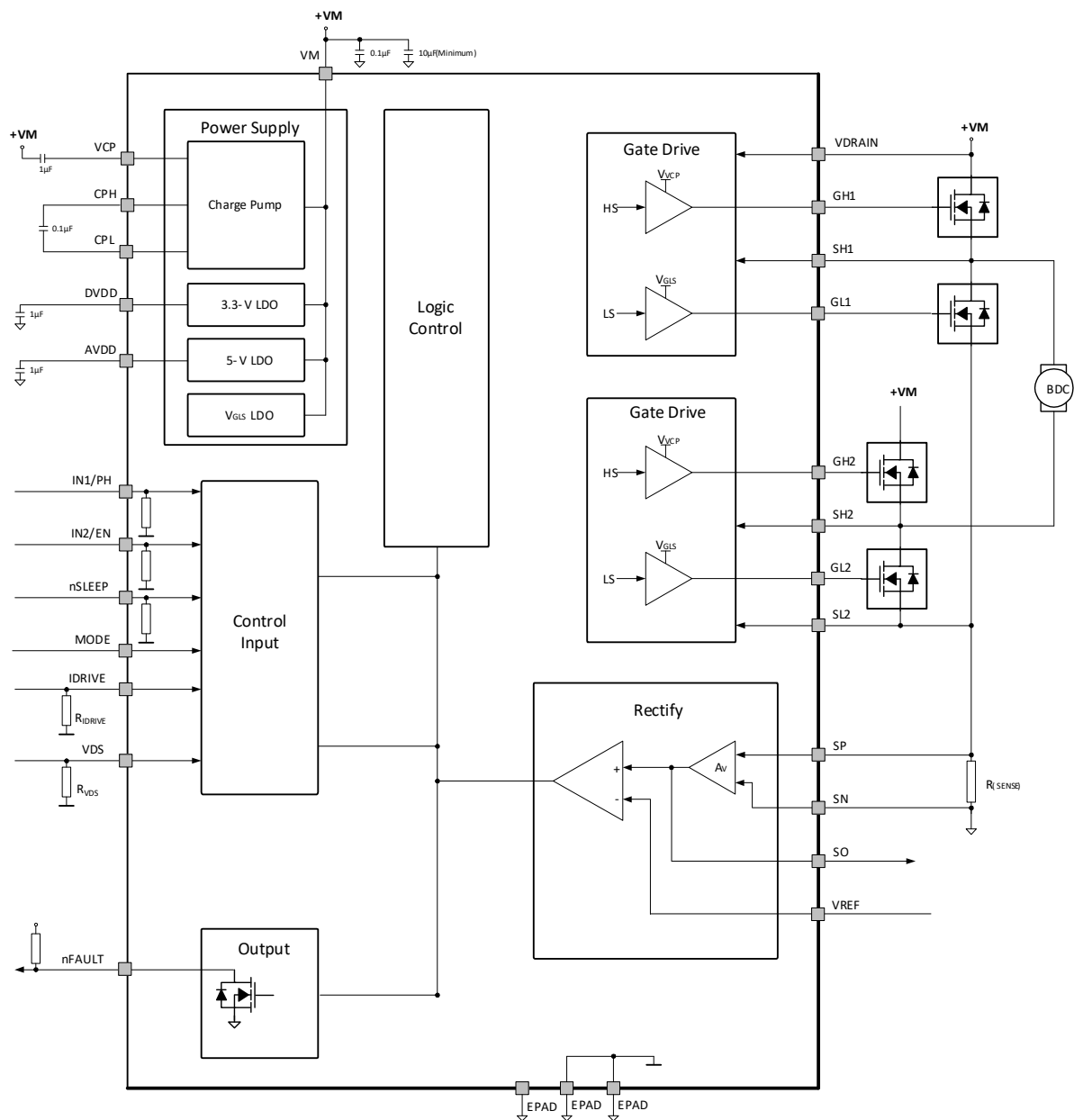| Part Number	Package	Marking
MS31702NA	QFN32	MS31702NA

TABLE of CONTENTS

PIN CONFIGURATION

PIN DESCRIPTION

Pin	Name	Type	Description
GND	1	-	Ground
IN1/PH	2	I	Input Control Pin. The logic of this pin depends on the MODE pin. This pin is connected to the ground with the internal pull-down resistor.
IN2/EN	3	I	Input Control Pin. The logic of this pin depends on the MODE pin. This pin is connected to the ground with the internal pull-down resistor.
GND	4	-	Ground
IDRIVE	5	I	Gate-drive Current Control Pin. The gate-drive current can be set by the resistance and voltage on this pin.
VDS	6	I	VDS Threshold Control Pin. VDS threshold can be set by the resistance and voltage on this pin.
GND	7	-	Ground
nSLEEP	8	I	Sleep-mode Input Pin. Pull this pin to logic low to make the device in low power-dissipation sleep mode with FET in high-impedance state (Hi-Z). The pin is connected to the ground with the internal pull-down resistor.
GND	9	-	Ground
nFAULT	10	O	Fault Indication Pin. When a fault occurs, this pin is pulled low. This pin is an open-drain output, which needs the external pull-up resistor.
MODE	11	I	Mode Control Pin. When the pin is pulled logic low, enabling EN/PH control mode. When the pin is pulled logic high, enabling independent H-bridge mode. When the pin is in no connection, enabling PWM control mode. When powering up or existing sleep mode, the pin operation is latched. The pin is connected to the internal pull-up and pull-down resistors.
DVDD	12	O	3.3V Logic Power Supply Output. The pin is connected to the ground with a 1µF bypass capacitor.
GND	13	-	Ground
AVDD	14	O	5V Analog Power Supply Output. The pin is connected to the ground with a 1µF bypass capacitor.
VREF	15	I	Analog Reference Voltage Input. The pin controls chopping current.

Pin	Name	Type	Description
SO	16	O	Shunt Amplifier Output. The capacitor on this pin cannot exceed 1nF.
GND	17	-	Ground.
GH1	18	O	High-side Gate. Connect this pin to high-side FET gate.
SH1	19	I	High-side Source. Connect this pin to high-side FET source.
GL1	20	O	Low-side Gate. Connect this pin to low-side FET gate.
SP	21	I	Positive Input of Shunt Amplifier. Connected to positive terminal of sense resistor.
SN	22	I	Negative Input of Shunt Amplifier. Connected to negative terminal of sense resistor.
SL2	23	I	Low-side Source. Connect this pin to low-side FET source.
GL2	24	O	Low-side Gate. Connect this pin to low-side FET gate.
SH2	25	I	High-side Source. Connect this pin to high-side FET source.
GH2	26	O	High-side Gate. Connect this pin to high-side FET gate.
VDRAIN	27	I	High-side Drain. Connect this pin to high-side FET drain.
VM	28	-	Power Supply. Connect this pin to the motor power supply. This pin is connected to the ground with a 0.1µF and the minimum 10µF bypass capacitors.
VCP	29	IO	Charge-pump Voltage. Connected to VM with a 1µF capacitor.
CPH	30	IO	Charge-pump Capacitor Output.
CPL	31	IO	Charge-pump Capacitor Input. Connected to CPH with a 0.1µF capacitor.
NC	32	-	No Connection.

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	VM	-0.3 ~ 47	V
Charge-pump Voltage	VCP, CPH	-0.3 ~ V_{VM}+12	V
Charge-pump Capacitor Input	CPL	-0.3 ~ V_{VM}	V
3.3V Logic Power Supply	DVDD	-0.3 ~ 3.8	V
5V Analog Power Supply	AVDD	-0.3 ~ 5.75	V
Voltage on Drain Pin	VDRAIN	-0.3 ~ 47	V
Voltage Difference between VM and VDRAIN	VM - VDRAIN	-10 ~ 10	V
Logic Control Pin Voltage	IN1, IN2, nSLEEP, nFAULT	-0.3 ~ 5.75	V
High-side Gate Pin Voltage	GH1, GH2	-0.3 ~ V_{VM}+12	V
Low-side Gate Pin Voltage	GL1, GL2	-0.3 ~ 12	V
High-side Source Pin Voltage	SH1, SH2	-1.2 ~ V_{VM}+1.2	V
Shunt Amplifier Input Pin Voltage	SP, SL2	-0.5 ~1.2	V
	SN	-0.3 ~0.3	V
Shunt Amplifier Output Pin Voltage	SO	-0.3 ~ 5.75	V
Shunt Amplifier Output Pin Current	SO	0 ~ 5	mA
VDRAIN Limit Current	VDRAIN	-2 ~ 2	mA
Open-drain Output Current	nFAULT	0 ~10	mA
Gate Pin Source Current	GH1, GL1, GH2, GL2	0 ~ 250	mA
Gate Pin Sink Current	GH1, GL1, GH2, GL2	0 ~ 500	mA
Junction Temperature	T_J	-40 ~150	°C
Storage Temperature	T_{STG}	-65 ~150	°C
ESD(HBM)		±3000	V
Thermal Resistance, Junction to Ambient	$R_{θJA}$	40	°C/W

RECOMMENDED OPERATING CONGITIONS

Parameter	Symbol	Range			Unit
		Min	Typ	Max	
Power Supply	V_{VM}	5.5		45	V
Logic Voltage	V_{CC}	0		5.25	V
Shunt Amplifier Reference Voltage	V_{VREF}	0.3[1]		3.6	V
PWM Frequency	$f_{(PWM)}$			100	kHz
5V Analog Power Supply Current	I_{AVDD}			30[2]	mA
3.3V Logic Power Supply Current	I_{DVDD}			30[2]	mA
Shunt Amplifier Output Current	I_{SO}			5	mA
Operating Temperature	T_A	-40		125	°C

Note:

1. V_{VREF} can be operated from 0 to 0.3V, but the accuracy is relatively low.

2. Power dissipation and thermal limit must be observed.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A=25°C, V_{VM}=13.5V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply (VM, AVDD, DVDD)						
VM Operating Voltage	V_{VM}	Gate Drive Function	5.5		45	V
		Logic Function	4.5		45	
VM Operating Current	I_{VM}	V_{VM}=13.5V, nSLEEP=1		6.0		mA
VM Sleep Current	$I_{(SLEEP)}$	nSLEEP=0,V_{VM}=13.5V,T_A=25°C		13		µA
		nSLEEP=0,V_{VM}=13.5V,T_A=125°C			30	
DVDD Output Voltage	V_{DVDD}	2mA Load		3.3		V
		30mA Load, V_{VM}=13.5V		3.2		
AVDD Output Voltage	V_{AVDD}	2mA Load		5.0		V
		30mA Load, V_{VM}=13.5V		5.0		
Charge Pump (VCP, CPH, CPL)						
VCP Operating Voltage	V_{VCP}	V_{VM}=13.5V		23.8		V
		V_{VM}=8V		14.7		
		V_{VM}=5.5V		9.7		
Charge-pump Current Capacity	I_{VCP}	V_{VM}>13.5V	9.5			mA
		8V<V_{VM}<13.5V	9.5			
		5.5V<V_{VM}<8V	7.5			
Control Inputs (IN1/PH, IN2/EN, nSLEEP, MODE)						
Logic Low Input Voltage	V_{IL}		0		0.8	V
Logic High Input Voltage	V_{IH}		1.5		5.25	V
Logic Input Hysteresis	V_{hys}		100			mV
Logic Low Input Current	I_{IL}	V_{IN}=0V, IN1/PH, IN2/EN, nSLEEP	-5		5	µA
		V_{IN}=0V, MODE			80	µA
Logic High Input Current	I_{IH}	V_{IN}=5V, IN1/PH, IN2/EN, nSLEEP			70	µA
		V_{IN}=5V, MODE			120	µA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Pull-down Resistance	R_{PD}	IN1/PH, IN2/EN, nSLEEP		100		kΩ
		MODE		55		kΩ
Pull-up Resistance	R_{PU}	MODE		26		kΩ
Control Outputs (nFAULT)						
Logic Low Output Voltage	V_{OL}	I_O=2mA			0.1	V
High-impedance Output Leakage Current	I_{OZ}	5V Pull-up Voltage	-2		2	µA
FET Gate Driver(GH1, GH2, SH1, SH2, GL1, GL2)						
High-side V_{GS} Gate Driver (Gate to Source)	V_{GSH}	V_{VM}>13.5V, Using SHx as a Reference		10.5	11.5	V
		V_{VM}=8V, Using SHx as a Reference	5.7		6.8	
		V_{VM}=5.5V, Using SHx as a Reference	3.4		4.3	
Low-side V_{GS} Gate Driver (Gate to Source)	V_{GSL}	V_{VM}>10.5V		10.5		
		V_{VM}<10.5V	V_{VM}-2			
High-side Source Current Peak(V_{VM}=13.5V)	I_{DRIVE} (SRC_HS)	$R_{(IDRIVE)}$<1kΩ to GND		14		mA
		$R_{(IDRIVE)}$=33kΩ to GND		28		
		$R_{(IDRIVE)}$=200kΩ to GND		65		
		$R_{(IDRIVE)}$>2MΩ to GND		183		
		$R_{(IDRIVE)}$=68kΩ to AVDD		221		
		$R_{(IDRIVE)}$=1kΩ to AVDD		248		
High-side Sink Current Peak(V_{VM}=13.5V)	I_{DRIVE} (SNK_HS)	$R_{(IDRIVE)}$<1kΩ to GND		21		mA
		$R_{(IDRIVE)}$=33kΩ to GND		41		
		$R_{(IDRIVE)}$=200kΩ to GND		99		
		$R_{(IDRIVE)}$>2MΩ to GND		252		
		$R_{(IDRIVE)}$=68kΩ to AVDD		322		
		$R_{(IDRIVE)}$=1kΩ to AVDD		383		

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low-side Source Current Peak(V_{VM}=13.5V)	I_{DRIVE} (SRC_LS)	R$_{(IDRIVE)}$<1kΩ to GND		10		mA
		R$_{(IDRIVE)}$=33kΩ to GND		20		
		R$_{(IDRIVE)}$=200kΩ to GND		49		
		R$_{(IDRIVE)}$>2MΩ to GND		132		
		R$_{(IDRIVE)}$=68kΩ to AVDD		179		
		R$_{(IDRIVE)}$=1kΩ to AVDD		230		
Low-side Sink Current Peak(V_{VM}=13.5V)	I_{DRIVE} (SNK_LS)	R$_{(IDRIVE)}$<1kΩ to GND		21		mA
		R$_{(IDRIVE)}$=33kΩ to GND		42		
		R$_{(IDRIVE)}$=200kΩ to GND		96		
		R$_{(IDRIVE)}$>2MΩ to GND		250		
		R$_{(IDRIVE)}$=68kΩ to AVDD		334		
		R$_{(IDRIVE)}$=1kΩ to AVDD		423		
FET Holding Current	I_{HOLD}	Pull-up current after t$_{DRIVE}$,GHx		10		mA
		Pull-up current after t$_{DRIVE}$, GLx		40		
FET Strong Pull-down Current	I_{STRONG}	GHx		750		mA
		GLx		1000		
FET Gate Holding Resistor	$R_{(OFF)}$	Pull-down GHx to SHx		150		kΩ
		Pull-down GLx to GND		150		
Shunt Amplifier and PWM Current Control (SP, SN, SO, VREF)						
VREF Input RMS Voltage	V_{VREF}	Used for Internal Chopping Current Control	0.3		3.6	V
VREF Input Impedance	R_{VREF}		1			MΩ
Amplifier Gain	A_V	60<V_{SP}<225mV, V_{SN}=GND		20		V/V
Input Offset Voltage	V_{IO}	V_{SP}=V_{SN}=GND		5	10	mV
Input Offset Voltage Temperature Drift	$V_{IO(DRIFT)}$	V_{SP}=V_{SN}=GND		10		µV/°C
SP Input Current	I_{SP}	V_{SP}=100mV, V_{SN}=GND		-50		µA
SO Output Voltage Range	V_{SO}		Av✕Vio		4.5	V
SO Pin Capacitance	$C_{(SO)}$				1	nF

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Protection Circuit						
VM Undervoltage Protection	$V_{(UVLO2)}$	VM Falling, UVLO2 Alarm Threshold		5.25		V
		VM Rising, UVLO2 Recovery Threshold		5.4		
VM Undervoltage Hysteresis	$V_{hys(UVLO)}$	Rising to falling	100			mV
Charge-pump Undervoltage Protection	$V_{(CP\_UV)}$	VCP Falling, CPUV Alarm Threshold		VM+1.5		V
		VCP Rising, CPUV Recovery Threshold		VM+1.55		
Charge-pump Undervoltage Hysteresis	$V_{hys(CP\_UV)}$	Rising to Falling		50		mV
V_{DS} Overcurrent Protection Threshold (V_{DS} of External FET)	$V_{DS(OCP)}$	$R_{(VDS)}$<1kΩ to GND		0.06		V
		$R_{(VDS)}$=33kΩ to GND		0.12		
		$R_{(VDS)}$=200kΩ to GND		0.24		
		$R_{(VDS)}$>2MΩ to GND		0.48		
		$R_{(VDS)}$=68kΩ to AVDD		0.96		
		$R_{(VDS)}$=1kΩ to AVDD		Disabled		
V_{SP} Overcurrent Protection Threshold, Measured by the Amplifier	$V_{SP(OCP)}$	V_{SP} relative to GND		1		V
Over-temperature Protection Temperature	T_{SD}		150			°C
Over-temperature Protection Hysteresis	T_{hys}			20		°C
Gate-drive Clamp Voltage	$V_{C(GS)}$	Positive Clamp Voltage		14		V
		Negative Clamp Voltage		-0.7		

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Switching Characteristics						
Power Supply (VM, AVDD, DVDD)						
Sleep Time	$t_{(SLEEP)}$	nSLEEP=0 to Sleep Start			110	µs
Wake-up Time	$t_{(wu)}$	nSLEEP=1 to Output Changes			1.1	ms
Turn-on Time	t_{on}	VM>UVLO2 to Output Changes			1.1	ms
Charge Pump (VCP, CPH, CPL)						
Charge-pump Switching Frequency	$f_{S(VCP)}$	VM>UVLO2	200	400	700	kHz
Control Input (IN1, IN2, nSLEEP, MODE, PH, EN)						
Propagation Delay	t_{pd}	IN1, IN2 to GHx or GLx		500		ns
FET Gate Driver (GH1, GH2, SH1, SH2, GL1, GL2)						
Dead Time	$t_{(DEAD)}$	The observed dead time depends on the IDRIVE pin setting.		260		ns
Gate Drive Time	$t_{(DRIVE)}$			2.75		µs
Shunt Amplifier and PWM Current Control (SP, SN, SO, VREF)						
Setup Time	t_S	V_{SP}=V_{SN}=GND to V_{SP}=120mV, V_{SN}=GND, A_V=20, $C_{(SO)}$=200pF			1	µs
PWM Off-time	t_{off}			27.5		µs
PWM Blanking Time	$t_{(BLANK)}$			2.2		µs
VM Undervoltage Detect Time	$t_{(UVLO)}$	VM Falling, UVLO Alarm		11		µs
Overcurrent Detect Time	$t_{(OCP)}$			4.4		µs
Overcurrent Off-time	$t_{(RETRY)}$			3.3		ms

FUNCTION DESCRIPTION

The MS31702NA controls four external NMOSFETs to drive bidirectional brushed DC motors. The MS31702NA can also be operated in independent H-bridge mode to drive two directional brushed DC motors. It supports power supply from 5.5V to 45V and enables low power-dissipation sleep mode through the nSLEEP pin. The control mode has three options, including configurable PH/EN, independent H-bridge control or PWM mode, which is easy to be connected with controller circuit.
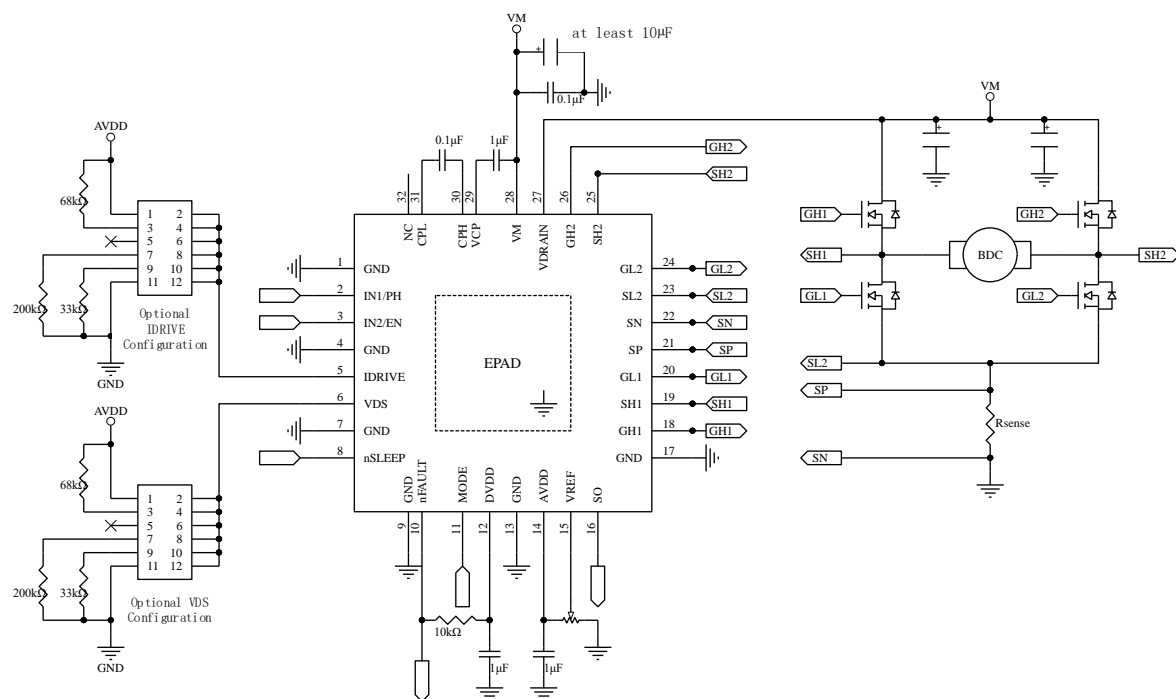
The MS31702NA can adjust gate drive strength or gate drive current to optimize different FET applications without external resistors. The device number of motor drive systems are significantly reduced by integrating the needed FET drive circuits into the single device. When VM voltage is more than 13.5V, high-side and low-side FETs are driven with 10.5V (nominal) gate source voltage (VGS). At lower VM voltage, the VGS is reduced. The high-side gate drive voltage is generated through a double-structure charge-pump that regulated to VM+10.5V.

The shunt amplifier gain of the MS31702NA is fixed at 20 times. The current can be limited by the current chopping way with internal fixed off-time.

The MS31702NA has complete protection functions, including: undervoltage lockout(UVLO), overcurrent protection(OCP), gate drive faults and thermal shutdown(TSD).
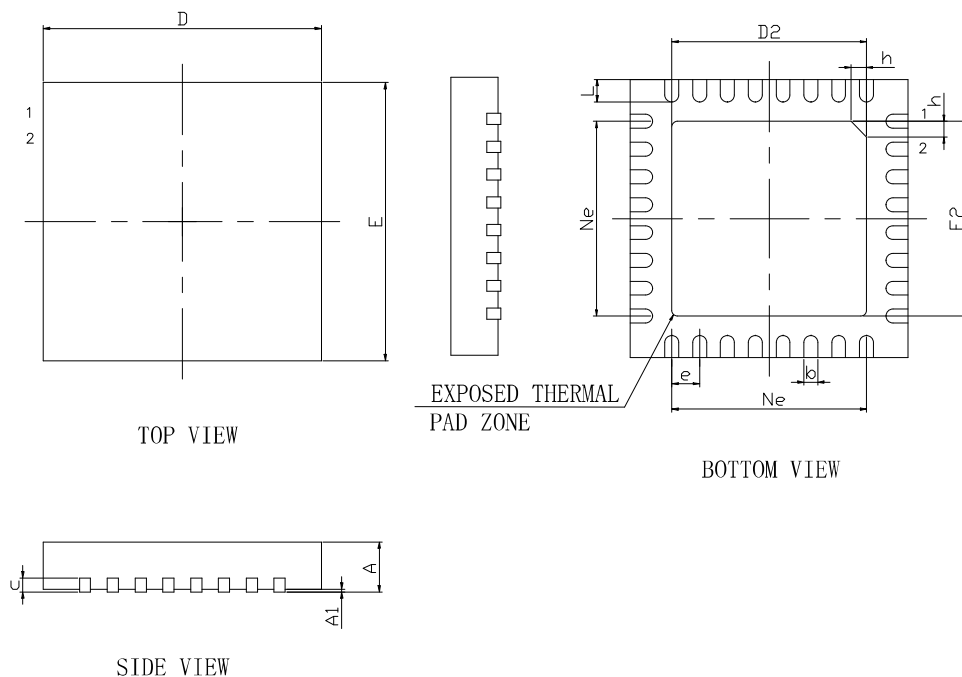
The MS31702NA integrates the spread spectrum clock function of internal digital oscillator and charge pumps, which is combined with output conversion rate to minimize radiation.

TYPICAL APPLICATION
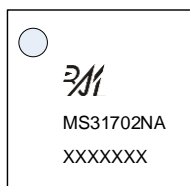
PACKAGE OUTLINE DIMENSIONS

QFN32

TOP VIEW

SIDE VIEW

EXPOSED THERMAL PAD ZONE

BOTTOM VIEW

Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description

Product Name: MS31702NA

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS31702NA	QFN32	1000	8	8000	4	32000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

  Customer should get latest version information and verify the integrity before placing order.

- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety

  standard and adopt corresponding precautions, in order to avoid personal injury and property loss

  caused by potential failure risk.

- The process of improving product is endless. And our company would sincerely provide more excellent

  product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken

to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.

2. The equipment shell must be grounded.

3. The tools used in the assembly process must be grounded.

4. Must use conductor packaging or anti-static materials packaging or transportation.

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