Analog Matrix Switch

PRODUCT DESCRIPTION

The MS3494 includes a 8×16 analog switch array, 7 to 128 address decoding and latch circuit. 128 switches can be addressed by differential address signals. Analog switch is on or off through “1” or “0” input logical level on DATA terminal. Analog signal ranges from VDD to VEE. In addition, switch array is allowed to be extended by CS pin.

PLCC44

FEATURES

- Control Latch, Address Decoding
- Short Setup Time and Hold Time
- Wide Voltage Range: 4.5V~13.2V
- 12Vpp Analog Signal
- R_{ON} Maximum 65Ω@V_{DD}=12V, 25°C
- R_{ON} ≤10Ω@V_{DD}=12V, 25°C
- Low Distortion, CMOS Switch
- Small Feedthrough and Crosstalk
- Dependent Analog Digital Reference Voltage Source

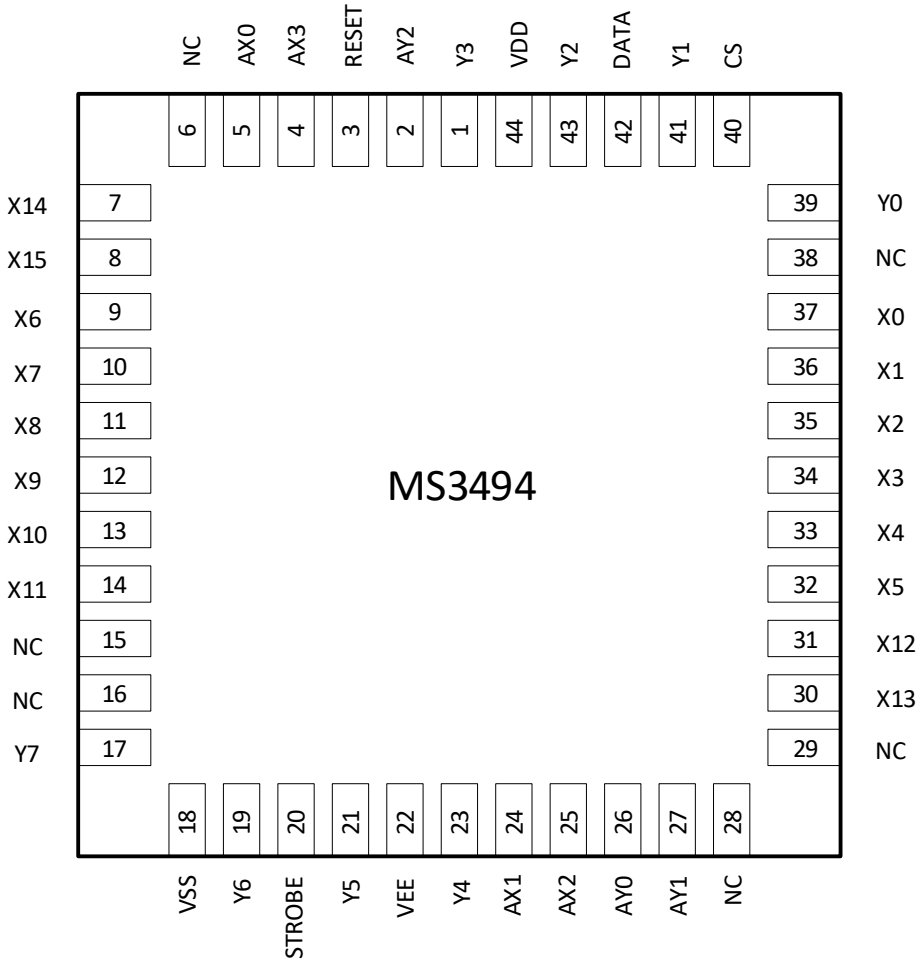
APPLICATIONS

- Key System
- PBX System
- Analog/Digital Multiple Switch
- Audio/Video Switch
- Mobile Device
- Test Device

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS3494	PLCC44	MS3494

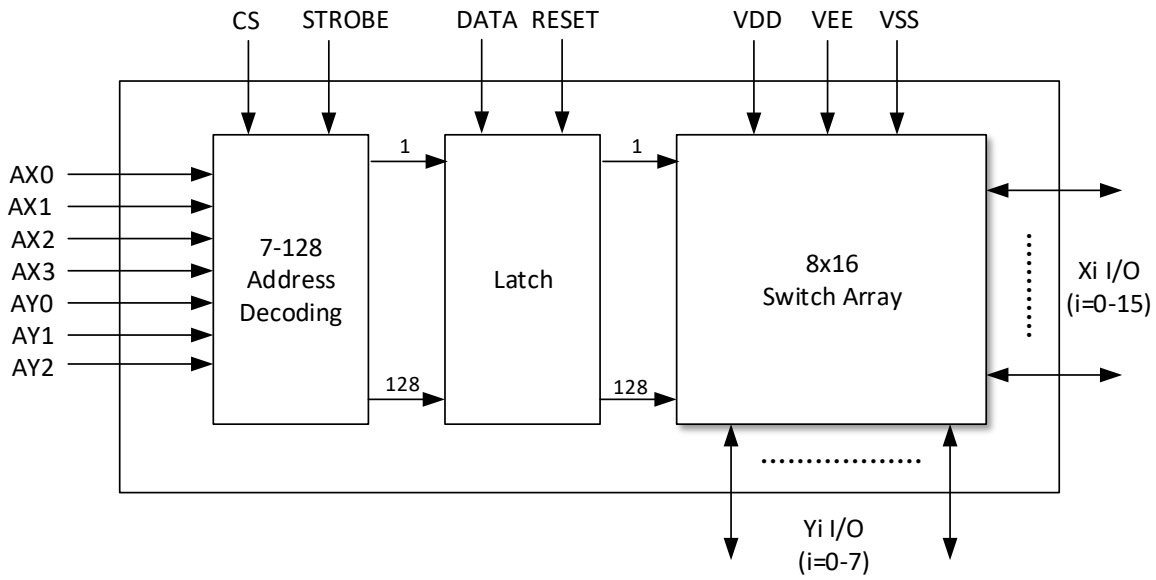
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	Y3	I/O	Analog Terminal Y3. Connect to Switch Array Y3
2	AY2	I	Address Line AY2
3	RESET	I	Close All Switches. Active High
4, 5	AX3, AX0	I	Address Line X3, X0
6	NC	-	Not Connection
7, 8	X14, X15	I/O	Analog Terminal X14, X15. Connect to Switch Array X14 and X15
9-14	X6-X11	I/O	Analog Terminal X6-X11. Connect to Switch Array X6-X11
15, 16	NC	-	Not Connection
17	Y7	I/O	Analog Terminal Y7. Connect to Switch Array Y7
18	VSS	-	Digital Ground
19	Y6	I/O	Analog Terminal Y6. Connect to Switch Array Y6
20	STROBE	I	Enable Address and Data. Before STROBE is high-level, address must remain stable; Before the falling edge of STROBE, DATA must remain stable. Active High
21	Y5	I/O	Analog Terminal Y5. Connect to Switch Array Y5
22	VEE	-	Negative Power Supply
23	Y4	I/O	Analog Terminal Y4. Connect to Switch Array Y4
24, 25	AX1, AX2	I	Address Line AX1 and AX2
26, 27	AY0, AY1	I	Address Line AY0 and AY1
28, 29	NC	-	Not Connection
30, 31	X13, X12	I/O	Analog Terminal X13 and X12. Connect to Switch Array X13 and X12
32-37	X5-X0	I/O	Analog Terminal X5-X0. Connect to Switch Array X5-X0
38	NC	-	Not Connection
39	Y0	I/O	Analog Terminal Y0. Connect to Switch Array Y0
40	CS	I	Chip Select. Active High
41	Y1	I/O	Analog Terminal Y1. Connect to Switch Array Y1
42	DATA	I	Data Input. Active High. When DATA is high-level, turn on switch; when DATA is low-level, turn off switch
43	Y2	I/O	Analog Terminal Y2. Connect to Switch Array Y2
44	VDD	-	Positive Power Supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	-0.3 ~ 16	V
	V_{SS}	-0.3 ~ V_{DD}+0.3	V
Analog Input Voltage	V_{INA}	-0.3 ~ V_{DD}+0.3	V
Digital Input Voltage	V_{IN}	V_{SS}-0.3 ~ V_{DD}+0.3	V
Port Current	I	±15	mA
Storage Temperature	T_{stg}	-65 ~ +150	°C
Power Dissipation	PD	0.6	W

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Ranges	Unit
Operating Temperature	T_A	-40 ~ 85	°C
Power Supply	V_{DD}	4.5 ~ 13.2	V
	V_{SS}	V_{EE} ~ V_{DD}-4.5	V
Analog Input Voltage	V_{INA}	V_{EE} ~ V_{DD}	V
Digital Input Voltage	V_{IN}	V_{SS} ~ V_{DD}	V

ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{EE}=V_{SS}=0V, V_{DD}=12V, T_A=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Quiescent Current	I_{DD}	All digital inputs V_{IN}=V_{SS} or V_{DD}		1	100	μA
		All digital inputs V_{IN}=2.4V+V_{SS}, V_{SS}=7.0V		0.4	1.5	mA
		All digital inputs V_{IN}=3.4V		5	15	mA
Leakage Current	I_{OFF}	/V_{xi}-V_{yj}/=V_{DD} - V_{EE}		±1	±500	nA
Input Low-level Voltage	V_{IL}	V_{SS}=6.5V, V_{EE}=0V			0.8+V_{SS}	V
Input High-level Voltage	V_{IH}	V_{SS}=6.5V, V_{EE}=0V	2+V_{SS}			V

DC Characteristics-On-Resistance

Parameter	Symbol	Condition		25°C		70°C		85°C		Unit
				Typ	Max	Typ	Max	Typ	Max	
On-Resistance	R_{ON}	V_{SS}=V_{EE}=0V, V_{DC}=V_{DC}/2, /V_{xi}-V_{yj}/=0.4V	V_{DD}=12V	45	65		75		80	Ω
			V_{DD}=10V	55	75		85		90	
			V_{DD}=5V	120	185		215		225	
On-Resistance Difference between Two Switches	ΔR_{ON}	V_{DD}=12V, V_{DC}=V_{DD}/2, V_{SS}=V_{EE}=0V, /V_{xi}-V_{yj}/=0.4V		5	10		10		10	Ω

AC Characteristics-Intersection Performance

V_{EE}=-7V, V_{DD}=5V, V_{SS}=0V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Switch Capacitance	C_S	f=1MHz		20		pF
Coupled Capacitance	C_F	f=1MHz		0.2		pF
Frequency Response Bandwidth, Channel "ON" 20log(V_{out}/V_{xi})=-3dB	F_{3dB}	Switch "ON", V_{INA}=2Vpp sine wave, R_L=1kΩ		45		MHz
Total Harmonic Distortion	THD	Switch "ON", V_{INA}=2Vpp, f=1kHz sine wave, R_L=1kΩ		0.01		%

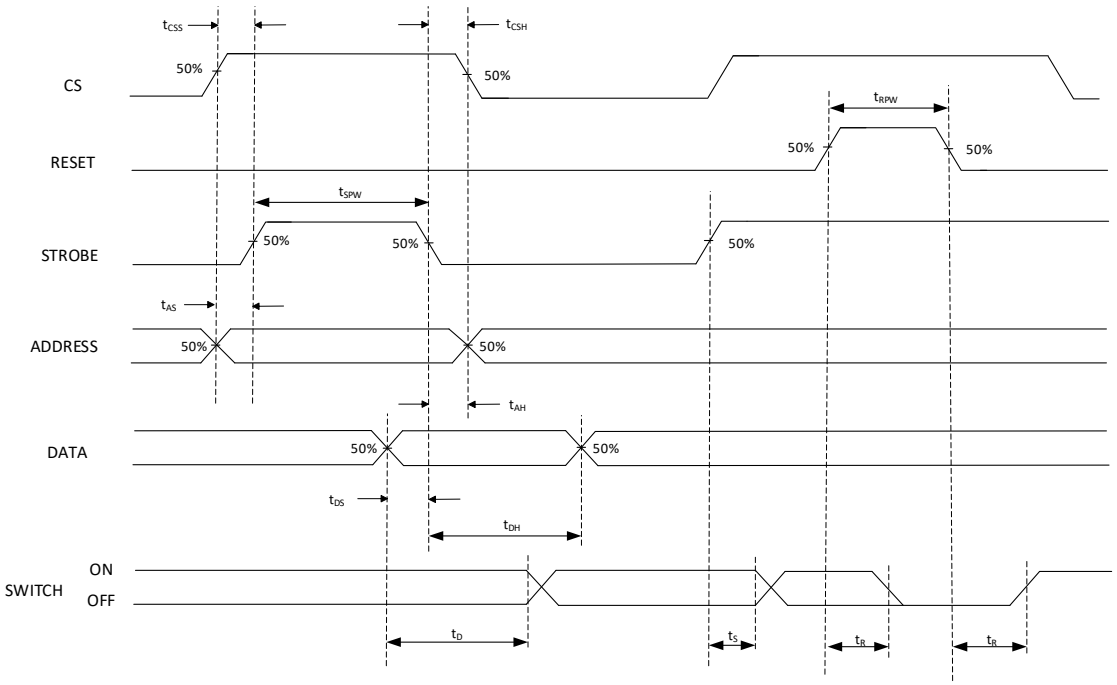
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Isolation, Channel "OFF"	FDT	All switches "OFF", V_{INA}=2Vpp, f=1kHz sine wave, R_L=1kΩ		-95		dB
Crosstalk between Two Channels	Xtalk	V_{INA}=2Vpp, f=10MHz sine wave, R_L=75Ω		-45		dB
		V_{INA}=2Vpp, f=10kHz sine wave, R_L=600Ω		-90		dB
		V_{INA}=2Vpp, f=10kHz sine wave, R_L=1kΩ		-85		dB
		V_{INA}=2Vpp, f=1kHz sine wave, R_L=10kΩ		-80		dB
Channel Delay	t_{ps}	R_L=1kΩ, C_L=50pF			30	ns

AC Characteristics-Timing

V_{EE}=-7V, V_{DD}=5V, V_{SS}=0V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Control Input Crosstalk to Switch (CS, DATA, ADDRES, STROBE)	CXtalk	V_{IN}=3V Square wave, R_{IN}=1kΩ, R_L=10kΩ		30		mVpp
Digital Input Capacitance	C_{DI}	f=1MHz		10		pF
Switch Frequency	f_O				20	MHz
Setup Time, DATA to STROBE	t_{DS}	R_L=1kΩ, C_L=50pF	10			ns
Hold Time, DATA to STROBE	t_{DH}	R_L=1kΩ, C_L=50pF	10			ns
Setup Time, ADDRES to STROBE	t_{AS}	R_L=1kΩ, C_L=50pF	10			ns
Hold Time, ADDRES to STROBE	t_{AH}	R_L=1kΩ, C_L=50pF	10			ns
Setup Time, CS to STROBE	t_{CSS}	R_L=1kΩ, C_L=50pF	10			ns
Hold Time, CS to STROBE	t_{CSH}	R_L=1kΩ, C_L=50pF	10			ns
STROBE Pulse Width	t_{SPW}	R_L=1kΩ, C_L=50pF	20			ns
RESET Pulse Width	t_{RPW}	R_L=1kΩ, C_L=50pF	40			ns
Delay, STROBE to Switch State	t_S	R_L=1kΩ, C_L=50pF		40	100	ns
Delay, DATA to Switch State	t_D	R_L=1kΩ, C_L=50pF		50	100	ns
Delay, RESET to Switch State	t_R	R_L=1kΩ, C_L=50pF		35	100	ns

Timing Diagram



FUNCTION DESCRIPTION

The MS3494 is a 8×16 analog switch matrix circuit. Switch matrix is 8 columns in Y direction and 16 rows in X direction. When switch is turned off, the corresponding X row and Y column could achieve absolute isolation. When switch is turned on, X row and Y column are connected.

Control register consists of a 128bit write RAM. Address input line (AX0-AX3, AY0-AY2) selects bit. Data is written to memory from DATA terminal. When STROBE and CS inputs are high-level, differential data can be written to DATA terminal. On the falling edge of STROBE, data is latched. In order to ensure valid write, data terminal must remain stable before falling edge. When logic "1" is written to memory unit, switch on the corresponding intersection; when logic "0" is written to memory unit, switch off the corresponding intersection. When data is written to memory, change the state of the intersection for addressed register, and other switches remain origin states. Writing differential data can achieve differential X and Y combinations. When RESET is logic "1", all switches are turned off and data in memory is cleared regardless of CS state. Two voltage reference pins (VSS and VEE) can provide negative analog signal. Digital signal voltage ranges from V_{DD} to V_{SS}. Analog signal voltage ranges from V_{DD} to V_{EE}. If only one power supply, VSS and VEE can be connected together.

Address Decoding

Under the control of STROBE and CS enable signal, seven address lines are input to 7-128 address decoder. DATA is buffered and as input for all memories. When RESET is low-level and CS is high-level, data and address can only be written to latch, and data is latched on the falling edge of STROBE. Only when STROBE is high-level, can only write data, and switch on and off. In order to ensure valid write, before the falling edge of STROBE, data should remain stable.

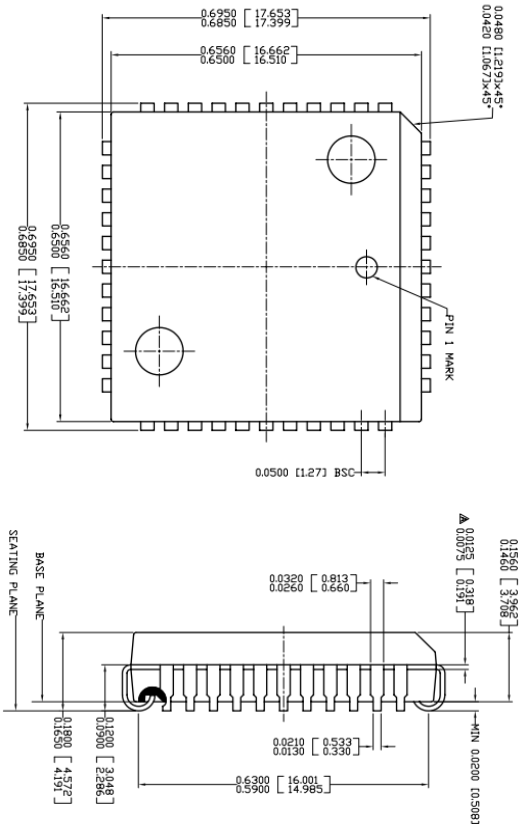
Address Decoding Truth Table

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	X12-Y0
1	1	1	0	0	0	0	X13-Y0
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0

1 0 1	0 1 1	1 1 1	1 1 1	0 0 0	0 0 0	0 0 0	X11-Y0 X14-Y0 X15-Y0
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	X0-Y1 ↓ X15-Y1
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	X0-Y2 ↓ X15-Y2
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	X0-Y3 ↓ X15-Y3
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	X0-Y4 ↓ X15-Y4
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	X0-Y5 ↓ X15-Y5
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	X0-Y6 ↓ X15-Y6
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	X0-Y7 ↓ X15-Y7

PACKAGE OUTLINE DIMENSIONS

PLCC44



MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description

Product Name: MS3494

Product Code: XXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Tube	Tube/Box	Piece/Box	Box/Carton	Piece/Carton
MS3494	PLCC44	30	70	2100	4	8400

STATEMENT

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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