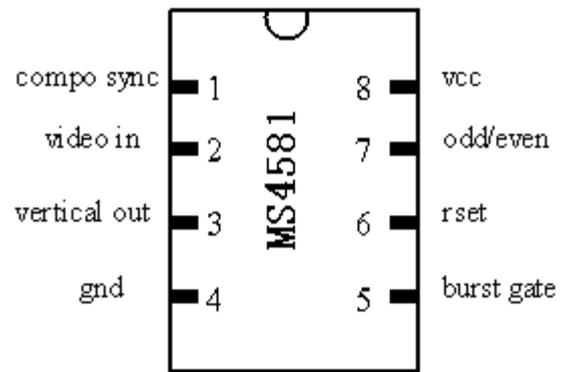


General Description

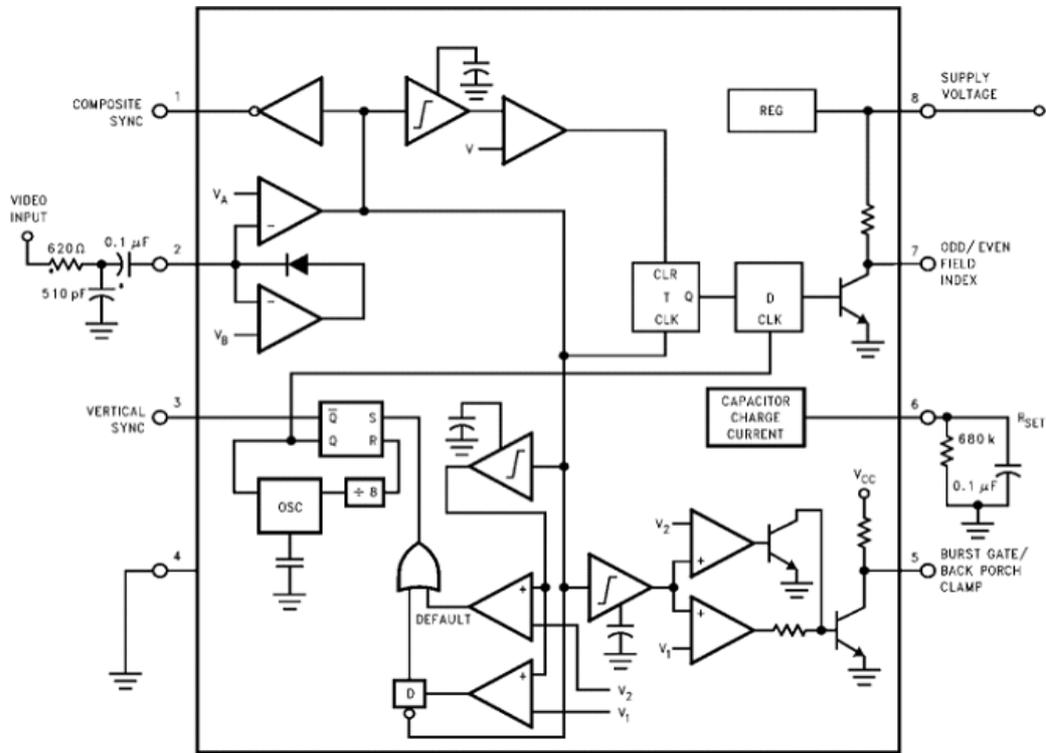
The MS4581 Video sync separator extracts timing information including composite and vertical sync, burst/back porch timing, and odd/even field information from standard negative going sync NTSC, PAL* and SECAM video signals with amplitude from 0.5V to 2V p-p. The integrated circuit is also capable of providing sync separation for non-standard, faster horizontal rate video signals. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default vertical output is produced after a time delay if the rising edge mentioned above does not occur within the externally set delay period, such as might be the case for a non-standard video signal.

Features

- 1) AC coupled composite input signal
- 2) >10 k Ω input resistance
- 3) <10 mA power supply drain current
- 4) Composite sync and vertical outputs
- 5) Odd/even field output
- 6) Burst gate/back porch output
- 7) Horizontal scan rates to 150 kHz
- 8) Edge triggered vertical output
- 9) Default triggered vertical output for non-standard video signal (video games-home computers)



Chip Frame:



(Figure 2)

Pin description:

Pin no.	Pin	name
1		composite sync
2		video input
3		vertical sync out
4		gnd
5		burst gate/back porch clamp
6		rset
7		odd/even
8		Vcc

Electrical Characteristics $V_{CC}=5V$; $R_{set}=680k$; $T_a=25^{\circ}C$

Parameter	Conditions		Min	Typ	Max	Units
Supply Current	Outputs at Logic 1	$V_{CC}=5V$ $V_{CC}=12V$		5.2 5.5	10 12	mA
DC Input Voltage	Pin 2		1.3	1.49	1.8	V
Input Threshold Voltage	(Note 1)		55	70	85	mV
Input Discharge Current	Pin 2; $V_{IN} = 2V$		6	10	16	μA
Input Clamp Charge Current	Pin 2; $V_{IN} = 1V$		0.2	1		mA
RSET Pin Reference Voltage	Pin 6; (Note 2)		1.10	1.26	1.35	V
Composite Sync. & Vertical Outputs	$I_{out}=40\mu A$; Logic1 $i_{out}=1.6 mA$ Logic1	$V_{CC}=5V$ $V_{CC}=12V$	4.0 11.0	4.5		V
		$V_{CC}=5V$ $V_{CC}=12V$	2.4 10			
Burst Gate & Odd/Even Outputs	$I_{out}=40\mu A$; Logic1	$V_{CC}=5V$ $V_{CC}=12V$	4.0 11.0	4		V
Composite Sync. Output	$I_{OUT} = -1.6 mA$; Logic 0; Pin 1			0.15	0.8	V
Vertical Sync. Output	$I_{OUT} = -1.6 mA$; Logic 0; Pin 3			0.15	0.8	V
Burst Gate Output	$I_{OUT} = -1.6 mA$; Logic 0; Pin 5			0.15	0.8	V
Odd/Even Output	$I_{OUT} = -1.6 mA$; Logic 0; Pin 7			0.2	0.8	V
Vertical Sync Width			190	237	300	μs
Burst Gate Width	2.7 k Ω from Pin 5 to V_{CC}		2.5	4	4.7	μs
Vertical Default Time	(Note 3)		32	58	90	μs

Note 1: Relative difference between the input clamp voltage and the minimum input voltage which produces a horizontal output pulse.

Note 2: Careful attention should be made to prevent parasitic capacitance coupling from any output pin (Pins 1, 3, 5 and 7) to the RSET pin (Pin 6).

Note 3: Delay time between the start of vertical sync (at input) and the vertical output pulse.

Absolute Maximum Ratings

Supply Voltage	13.2V	Max
Input Voltage Vpp	3V (Vcc=5V) 6V (Vcc ≥ 8V)	Max
Output Sink Currents; Pins, 1, 3, 5	5mA	Max
Output Sink Current; Pin 7	2mA	Max
Operation Temperature Range	-30°C ~ 80°C	
Storage Temperature Range	-65°C ~ +150°C	
ESD Susceptibility	2kV	Human body model

Application Notes:

The MS4581 is designed to strip the synchronization signals from composite video sources that are in, or similar to, the N.T.S.C. format. Input signals with positive polarity video (increasing signal voltage signifies increasing scene brightness) from 0.5V (p-p) to 2V (p-p) can be accommodated. The MS4581 operates from a single supply voltage between 5V DC and 12V DC. The only required external components besides a power supply decoupling capacitor at pin 8 and a set current decoupling capacitor at pin 6, are the composite input coupling capacitor at pin 2 and one resistor at pin 6 that sets internal current levels. The resistor on pin 6 (i.e. Rset) allows the MS4581 to be adjusted for source signals with line scan frequencies differing from 15.734 kHz. Four major sync signals are available from the I/C; composite sync including both horizontal and vertical scan timing information; a vertical sync pulse; a burst gate or back porch clamp pulse; and an odd/even output. The odd/even output level identifies which video field of an interlaced video source is present at the input. The outputs from the MS4581 can be used to gen-lock video camera/VTR signals with graphics sources, provide identification of video fields for memory storage, recover suppressed or contaminated sync signals, and provide timing references for the extraction of coded or uncoded data on specific video scan lines. To better understand the MS4581 timing information and the type of signals that are used, refer to Figure 2(a-e) which shows a portion of the composite video signal from the end of one field through the beginning of the next field.

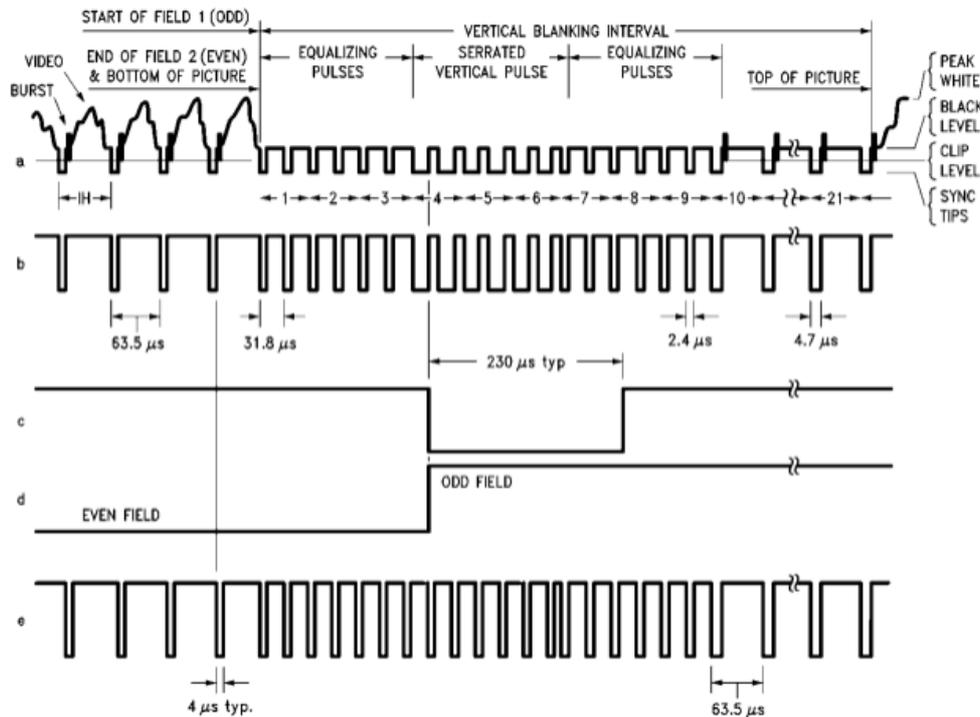


FIGURE 2. (a) Composite Video; (b) Composite Sync; (c) Vertical Output Pulse; (d) Odd/Even Field Index; (e) Burst Gate/Back Porch Clamp

COMPOSITE SYNC OUTPUT

The composite sync output, Figure 2(b), is simply a reproduction of the signal waveform below the composite video black level, with the video completely removed. This is obtained by clamping the video signal sync tips to 1.5V DC at Pin 2 and using a comparator threshold set just above this voltage to strip the sync signal, which is then buffered out to Pin 1. The threshold separation from the clamped sync tip is nominally 70 mV which means that for the minimum input level of 0.5V (p-p), the clipping level is close to the halfway point on the sync pulse amplitude (shown by the dashed line on Figure 2(a)). This threshold separation is independent of the signal amplitude, therefore, for a 2V (p-p) input the clipping level occurs at 11% of the sync pulse amplitude. The charging current for the input coupling capacitor is 0.8 mA, Normally the signal source for the MS4581 is assumed to be clean and relatively noise-free, but some sources may have excessive video peaking, causing high frequency video and chroma components to extend below the black level reference. Some video discs keep the chroma burst pulse present throughout the vertical blanking period so that the burst actually appears on the sync tips for three line periods instead of at black level. A clean composite sync signal can be generated from these sources by filtering the input signal. When the source impedance is low, typically 75 Ω , a 620 Ω resistor in series with the source and a 510 pF capacitor to ground will form a low pass filter with a corner frequency of 500 kHz. This bandwidth is more than sufficient to pass the sync pulse portion of the waveform; however, any subcarrier content in the signal will be attenuated by almost 18 dB,

effectively taking it below the comparator threshold. Filtering will also help if the source is contaminated with thermal noise. The output waveforms will become delayed from between 40 ns to as much as 200 ns due to this filter. This much delay will not usually be significant but it does contribute to the sync delay produced by any additional signal processing. Since the original video may also undergo processing, the need for time delay correction will depend on the total system, not just the sync stripper.

VERTICAL SYNC OUTPUT

A vertical sync output is derived by internally integrating the composite sync waveform (Figure 1). To understand the generation of the vertical sync pulse, refer to the lower left hand section Figure 1. Note that there are two comparators in the section. One comparator has an internally generated voltage reference called V1 going to one of its inputs. The other comparator has an internally generated voltage reference called V2 going to one of its inputs. Both comparators have a common input at their noninverting input coming from the internal integrator. The internal integrator is used for integrating the composite sync signal. This signal comes from the input side of the composite sync buffer and are positive going sync pulses. The capacitor to the integrator is internal to the MS4581. The capacitor charge current is set by the value of the external resistor RSET. The output of the integrator is going to be at a low voltage during the normal horizontal lines because the integrator has a very short time to charge the capacitor, which is during the horizontal sync period. The equalization pulses will keep the output voltage of the integrator at about the same level, below the V1. During the vertical sync period the narrow going positive pulses shown in Figure 2 is called the serration pulse. The wide negative portion of the vertical sync period is called the vertical sync pulse. At the start of the vertical sync period, before the first Serration pulse occurs, the integrator now charges the capacitor to a much higher voltage. At the first serration pulse the integrator output should be between V1 and V2. This would give a high level at the output of the comparator with V1 as one of its inputs. This high is clocked into the “D” flip-flop by the falling edge of the serration pulse (remember the sync signal is inverted in this section of the MS4581). The “Q” output of the “D” flip-flop goes through the OR gate, and sets the R/S flip-flop. The output of the R/S flip-flop enables the internal oscillator and also clocks the ODD/EVEN “D” flip-flop. The ODD/EVEN field pulse operation is covered in the next section. The output of the oscillator goes to a divide by 8 circuit, thus resetting the R/S flip-flop after 8 cycles of the oscillator. The frequency of the oscillator is established by the internal capacitor going to the oscillator and the external RSET. The “Q” output of the R/S flip-flop goes to pin 3 and is the actual vertical sync output of the MS4581. By clocking the “D” flip-flop at the start of the first serration pulse means that the vertical sync output pulse starts at this point in time and lasts for eight cycles of the internal oscillator as shown in Figure 2. How RSET affects the integrator and the internal oscillator is shown under the Typical Performance Characteristics. The first graph is “RSET Value Selection vs Vertical Serration Pulse Separation”. For

this graph to be valid, the vertical sync pulse should last for at least 85% of the horizontal half line (47% of a full horizontal line). A vertical sync pulse from any standard should meet this requirement; both NTSC and PAL do meet this requirement (the serration pulse is the remainder of the period, 10% to 15% of the horizontal half line). Remember this pulse is a positive pulse at the integrator but negative in Figure 2. This graph shows how long it takes the integrator to charge its internal capacitor above V1. With RSET too large the charging current of the integrator will be too small to charge the capacitor above V1, thus there will be no vertical sync output pulse. As mentioned above, RSET also sets the frequency of the internal oscillator. If the oscillator runs too fast its eight cycles will be shorter than the vertical sync portion of the composite sync. Under this condition another vertical sync pulse can be generated on one of the later serration pulse after the divide by 8 circuit resets the R/S flip-flop. The first graph also shows the minimum RSET necessary to prevent a double vertical pulse, assuming that the serration pulses last for only three full horizontal line periods (six serration pulses for NTSC). The actual pulse width of the vertical sync pulse is shown in the “Vertical Pulse Width vs RSET” graph. Using NTSC as an example, lets see how these two graphs relate to each other. The Horizontal line is 64 μs long, or 32 μs for a horizontal half line. Now round this off to 30 μs . In the “RSET Value Selection vs Vertical Serration Pulse Separation” graph the minimum resistor value for 30 μs serration pulse separation is about 550 Kohm. Going to the “Vertical Pulse Width vs RSET” graph one can see that 550 Kohm gives a vertical pulse width of about 180 μs , the total time for the vertical sync period of NTSC (3 horizontal lines). A 550 Kohm will set the internal oscillator to a frequency such that eight cycles gives a time of 180 μs , just long enough to prevent a double vertical sync pulse at the vertical sync output of the MS4581. The MS4581 also generates a default vertical sync pulse when the vertical sync period is unusually long and has no serration pulses. With a very long vertical sync time the integrator has time to charge its internal capacitor above the voltage level V2. Since there is no falling edge at the end of a serration pulse to clock the “D” flip-flop, the only high signal going to the OR gate is from the default comparator when output of the integrator reaches V2. At this time the R/S flip-flop is toggled by the default comparator, starting the vertical sync pulse at pin 3 of the MS4581. If the default vertical sync period ends before the end of the input vertical sync period, then the falling edge of the vertical sync (positive pulse at the “D” flip-flop) will clock the high output from the comparator with V1 as a reference input. This will retrigger the oscillator, generating a second vertical sync output pulse. The “Vertical Default Sync Delay Time vs RSET” graph shows the relationship between the RSET value and the delay time from the start of the vertical sync period before the default vertical sync pulse is generated. Using the NTSC example again the smallest resistor for RSET is 500 Kohm. The vertical default time delay is about 50 μs , much longer than the 30 μs serration pulse spacing. A common question is how can one calculate the required RSET with a video timing standard that has no serration pulses during the vertical blanking. If the default vertical sync is to be used this is a very easy task. Use the

“Vertical Default Sync Delay Time vs RSET” graph to select the necessary RSET to give the desired delay time for the vertical sync output signal. If a second pulse is undesirable, then check the “Vertical Pulse Width vs RSET” graph to make sure the vertical output pulse will extend beyond the end of the input vertical sync period. In most systems the end of the vertical sync period may be very accurate. In this case the preferred design may be to start the vertical sync pulse at the end of the vertical sync period, similar to starting the vertical sync pulse after the first serration pulse. A VGA standard is to be used as an example to show how this is done. In this standard a horizontal line is 32 μs long. The vertical sync period is two horizontal lines long, or 64 μs . The vertical default sync delay time must be longer than the vertical sync period of 64 μs . In this case RSET must be larger than 680 Kohm. RSET must still be small enough for the output of the integrator to reach V1 before the end of the vertical period of the input pulse. The first graph can be used to confirm that RSET is small enough for the integrator. Instead of using the vertical serration pulse separation, use the actual pulse width of the vertical sync period, or 64 μs in this example. This graph is linear, meaning that a value as large as 2.7 MOHM can be used for RSET (twice the value as the maximum at 30 μs). Due to leakage currents it is advisable to keep the value of RSET under 2.0 Mohm. In this example a value of 1.0 Mohm is selected, well above the minimum of 680 Kohm. With this value for RSET the pulse width of the vertical sync output pulse of the MS4581 is about 340 μs .

ODD/EVEN FIELD PULSE

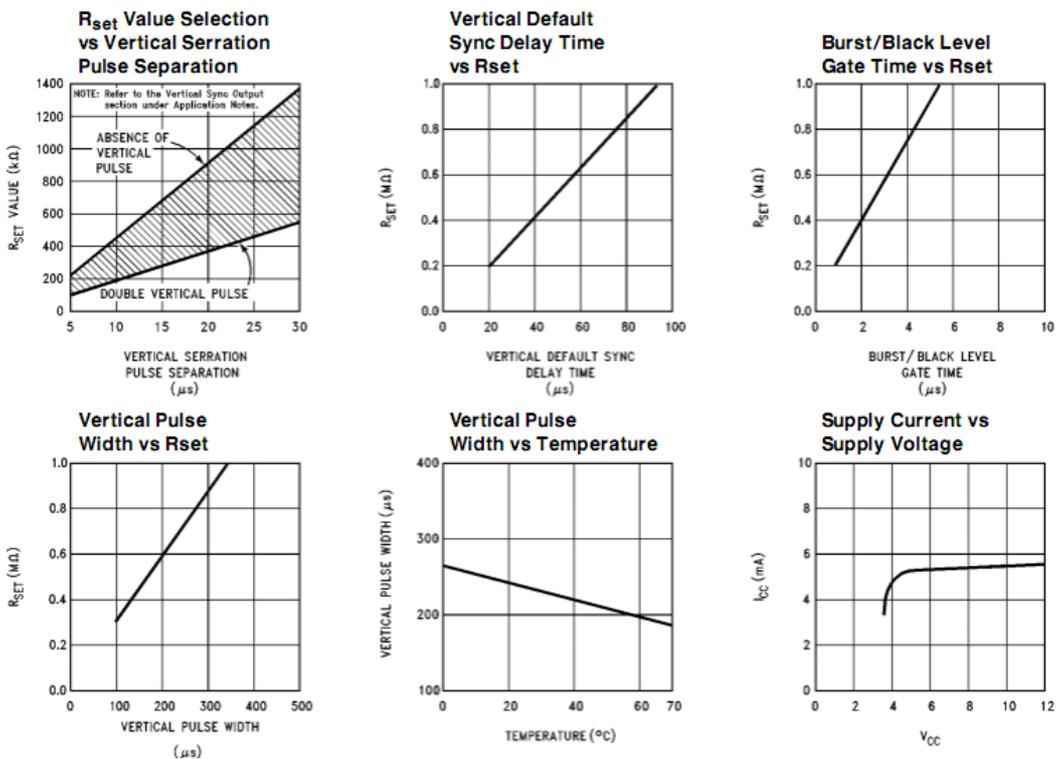
An unusual feature of MS4581 is an output level from Pin 7 that identifies the video field present at the input to the MS4581. This can be useful in frame memory storage applications or in extracting test signals that occur in alternate fields. For a composite video signal that is interlaced, one of the two fields that make up each video frame or picture must have a half horizontal scan line period at the end of the vertical scan—i.e., at the bottom of the picture. This is called the “odd field” or “even field”. The “even field” or “field 2” has a complete horizontal scan line at the end of the field. An odd field starts on the leading edge of the first equalizing pulse, whereas the even field starts on the leading edge of the second equalizing pulse of the vertical retrace interval. Figure 2(a) shows the end of the even field and the start of the odd field. To detect the odd/even fields the MS4581 again integrates the composite sync waveform (Figure 1). A capacitor is charged during the period between sync pulses and discharged when the sync pulse is present. The period between normal horizontal sync pulses is enough to allow the capacitor voltage to reach a threshold level of a comparator that clears a flip-flop which is also being clocked by the sync waveform. When the vertical interval is reached, the shorter integration time between equalizing pulses prevents this threshold from being reached and the Q output of the flip-flop is toggled with each equalizing pulse. Since the half line period at the end of the odd field will have the same effect as an equalizing pulse period, the Q output will have a different polarity on successive fields. Thus by comparing the Q polarity with the vertical output pulse, an odd/even field index is generated. Pin 7 remains low during

the even field and high during the odd field.

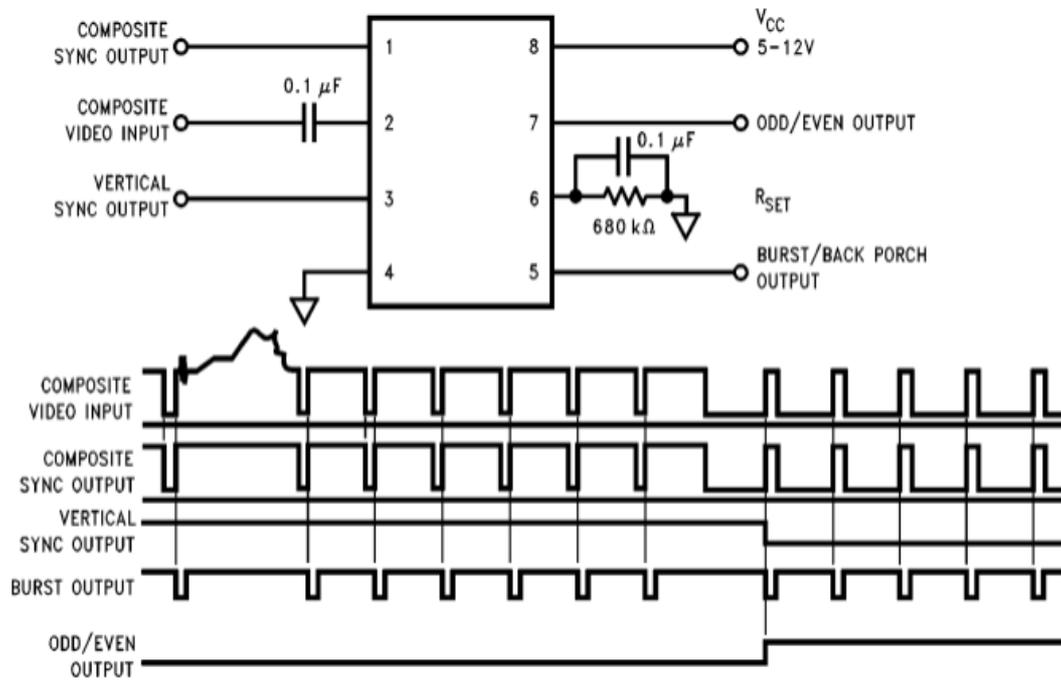
BURST/BACKPORCH OUTPUT PULSE

In a composite video signal, the chroma burst is located on the backporch of the horizontal blanking period. This period, approximately 4.8 μs long, is also the black level reference for the subsequent video scan line. The MS4581 generates a pulse at Pin 5 that can be used either to retrieve the chroma burst from the composite video signal (thus providing a subcarrier synchronizing signal) or as a clamp for the DC restoration of the video waveform. This output is obtained simply by charging an internal capacitor starting on the trailing edge of the horizontal sync pulses. Simultaneously the output of Pin 5 is pulled low and held until the capacitor charge circuit times out—4 μs later. A shorter output burst gate pulse can be derived by differentiating the burst output using a series C-R network. This may be necessary in applications which require high horizontal scan rates in combination with normal (60 Hz–120 Hz) vertical scan rates.

Typical Performance Characteristics



Connection Diagram



Physical Dimensions

