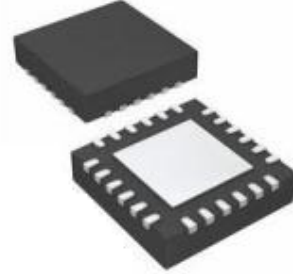


Single-Channel, Ultra-Low Noise, 256 Microstepping, Low-Voltage Motor Driver

PRODUCT DESCRIPTION

The MS41939 is single-channel, 5V low-voltage stepper motor driver. Ultra-low noise microstepping could be realized by voltage driving method with current microstepping and torque ripple correction technology.

The MS41939 has a built-in DC motor driver and the output resistance is low to 1.1Ω.



QFN24

FEATURES

- Voltage Driving Method, 256 Microstepping (Single-channel)
Maximum Driving Current $\pm 0.5A$ for Each H-Bridge
- 4-Wire SPI Communication
- Built-in DC Motor Drive, Maximum Driving Current $\pm 0.5A$
- QFN24 Package (Back Thermal Pad)

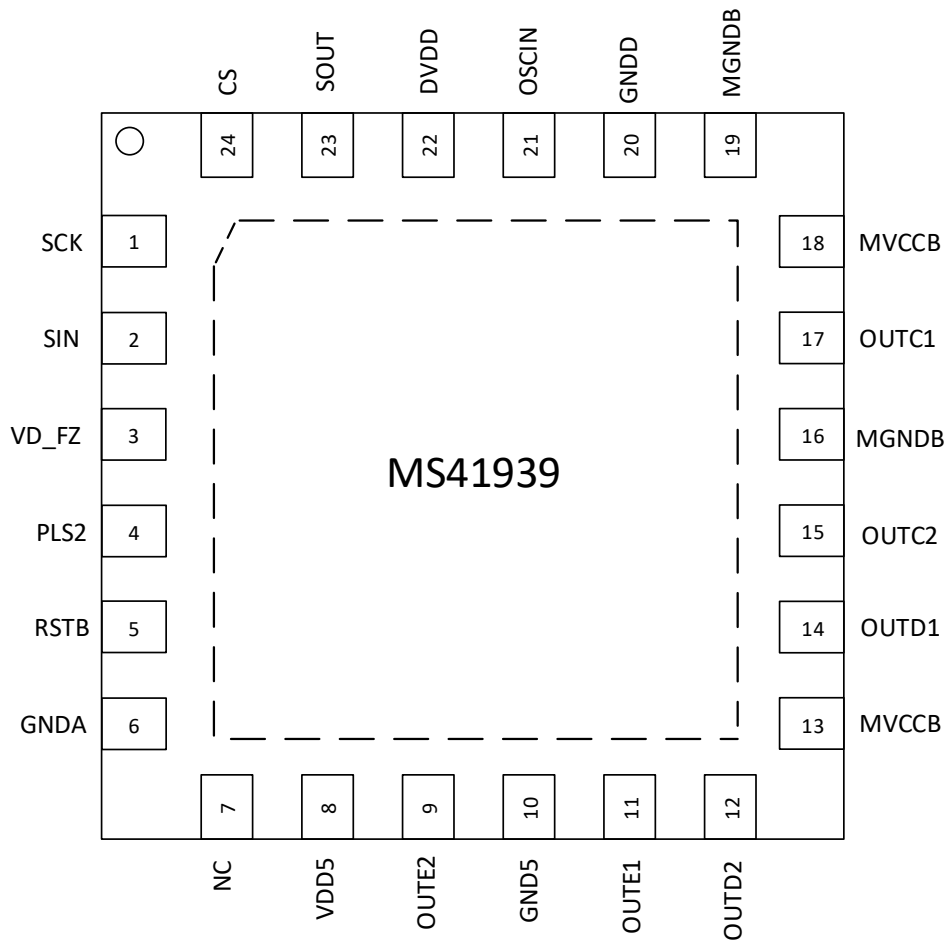
APPLICATIONS

- Robot, Precision Industry Device
- Camera
- Monitoring Camera

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS41939	QFN24	MS41939

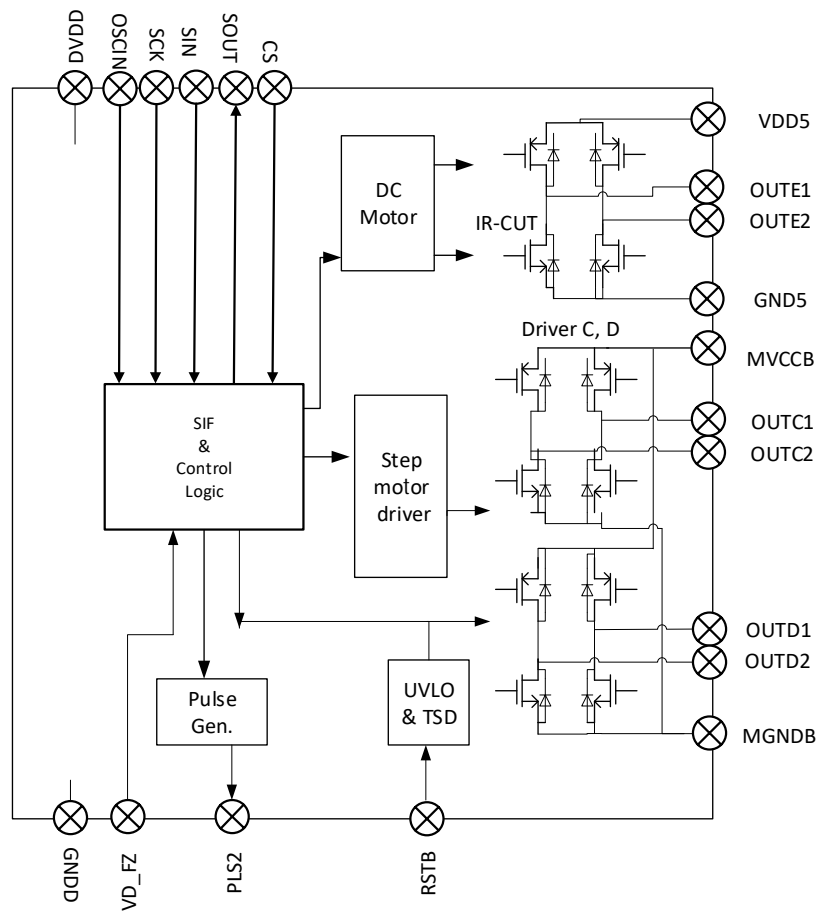
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	SCK	I	Serial Clock Input
2	SIN	I	Serial Data Input
3	VD_FZ	I	Stepper Motor Driver, Synchronous Signal Input
4	PLS2	O	Pulse 2 Output
5	RSTB	I	Reset Signal Input
6	GNDA	-	Analog GND
7	NC	-	Not Connection
8	VDD5	-	DC Motor Power Supply E
9	OUTE2	O	Motor Output E2
10	GND5	-	DC Motor Ground E
11	OUTE1	O	Motor Output E1
12	OUTD2	O	Motor Output D2
13	MVCCB	-	5V Motor Power Supply B
14	OUTD1	O	Motor Output D1
15	OUTC2	O	Motor Output C2
16	MGNDB	-	Motor GNDB
17	OUTC1	O	Motor Output C1
18	MVCCB	-	5V Motor Power Supply B
19	MGNDB	-	Motor GND B
20	GNDD	-	Digital GND
21	OSCIN	I	OSCIN Input
22	DVDD	-	3V Digital Power Supply
23	SOUT	O	Serial Data Output
24	CS	I	Chip Select Input

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Ratings

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Ratings	Unit
Power Supply, Analog and Control Part ¹	DVDD	-0.3 ~ +4.0	V
Power Supply, Motor Control 1 ¹	MVCCB VDD5	-0.3 ~ +6.0	V
Power Dissipation ²	P _D	141.1	mW
Operating Temperature ³	T _A	-40 ~ +100	°C
Storage Temperature ³	T _{STG}	-65 ~ +150	°C
Junction Temperature	T _J	-40 ~ +150	°C
Stepper Motor, H-Bridge Drive Current	I _{M1(CD)}	±0.5	A/ch
Instantaneous H-Bridge Drive Current	I _{M(pluse)}	±0.6	A/ch
Input Voltage, Digital Part ⁴	V _{IN}	-0.3 ~ (DVDD + 0.3)	V
Total Current ⁵	I _{totalmax}	0.8	A
ESD (HBM)	V _{ESD}	>±3k	V

Note:

1. Absolute maximum ratings are used in the range of power dissipation.
2. Power dissipation refers to the value of encapsulated monomer at T_A=85°C. In practice, it is expected to refer to the technical data and P_D-T_A characteristic diagram on the basis of power supply, load, ambient temperature conditions, and then carry out the heat dissipation design which does not exceed the power dissipation value.
3. Except power dissipation, ambient temperature and storage temperature parameters, all parameters are at T_A=25°C.
4. (DVDD+0.3) voltage shall not exceed 4.0V.
5. The constant average total current shouldn't exceed 0.8A for thermal performance. If the current is more than 0.8A, the demand for PCB would be higher.

Operating Power Supply

Parameter	Symbol	Range			Unit
		Min	Typ	Max	
Power Supply	DVDD	2.7	3.3	3.6	V
	MVCCB	3.0	5	5.5	

Terminal Tolerance Current and Voltage Ranges

Note: 1. The parameters cannot exceed the absolute maximum ratings in any conditions.

2. Rated voltage value refers to each terminal voltage with respect to GND. GND is the voltage of GNDA, GNDD, MGNDB, MGNDE. GND = GNDD = MGNDB = GND5.

3. 3V power is the voltage of DVDD.

4. Outside input voltage and current are strictly prohibited except the described terminals below.

5. For the current, "+" means the current flowing to IC, and "-" means the current flowing out from IC.

Pin	Name	Range	Unit
21	OSCIN	-0.3 ~ (DVDD + 0.3)	V
24	CS	-0.3 ~ (DVDD + 0.3)	V
1	SCK	-0.3 ~ (DVDD + 0.3)	V
2	SIN	-0.3 ~ (DVDD + 0.3)	V
3	VD_FZ	-0.3 ~ (DVDD + 0.3)	V
5	RSTB	-0.3 ~ (DVDD + 0.3)	V
12	OUTD2	±0.5	A
14	OUTD1	±0.5	A
15	OUTC2	±0.5	A
17	OUTC1	±0.5	A
11	OUTE1	±0.5	A
9	OUTE2	±0.5	A

Note: (AVDD+0.3) voltage should not exceed 4.0V. (DVDD+0.3) voltage should not exceed 4.0V.

ELECTRICAL CHARACTERISTICS

MVCCB = VDD5 = 5V, DVDD = 3.3V. Unless other noted, $T_A = 25^{\circ}\text{C} \pm 2^{\circ}\text{C}$.

Current Consumption

Parameter	Symbol	Condition	Min	Typ	Max	Unit
MVCCB Power Supply Current when Reset	I_{omisable}	Output Open-circuit, 27MHz Input		0		μA
MVCCB Power Supply Current when Enable	I_{menable}	Output Open-circuit, 27MHz Input		0.3		mA
3V Power Supply Current when Reset	I_{cc3reset}	Output Open-circuit, 27MHz Input		100		μA
3V Power Supply Current when Enable	$I_{\text{cc3enable}}$	Output Open-circuit, 27MHz Input		2.5		mA
Power Supply Current when Standby	$I_{\text{ccstandby}}$	RSTB = High Output Open-circuit, 27MHz Input, Total Current		4		mA
Power Supply Current when FZ = Enable	I_{CCps}	RSTB = High Output Open-circuit, 27MHz Input, FZ = Enable, Total Current		5		mA

Digital Input and Output

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input Voltage	$V_{\text{in(H)}}$	RSTB	$0.54 \times \text{DVDD}$		$\text{DVDD} + 0.3$	V
Low-level Input Voltage	$V_{\text{in(L)}}$	RSTB	-0.3		$0.25 \times \text{DVDD}$	V
SOUT High-level Output	$V_{\text{out(H)}}$	$I_{\text{OUT}} = 1\text{mA}$	$\text{DVDD} - 0.5$			V
SOUT Low-level Output	$V_{\text{out(L)}}$	$I_{\text{OUT}} = 1\text{mA}$			0.5	V
PLS2 High-level Output	$V_{\text{out(H)}}$		$0.9 \times \text{DVDD}$			V
PLS2 Low-level Output	$V_{\text{out(L)}}$				$0.1 \times \text{DVDD}$	V
Input Pull-down Impedance	R_{pullret}	RSTB		100		k Ω

Stepper Motor Driver

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-side On Resistance	R _{onFZHS}	I _M = 200mA		0.8		Ω
Low-side On Resistance	R _{onFZLS}	I _M = 200mA		0.7		Ω
H-Bridge Leakage Current	I _{leakFZ}				1	μA

DC Motor Driver (DRIVER E, IR-CUT in Camera)

Unless other noted, VDD5=5V, R_L=20Ω, T_A=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-side On Resistance	R _{oncutH}	I _{outE} =200mA		0.8		Ω
Low-side On Resistance	R _{oncutL}	I _{outE} =200mA		0.45		
Output Leakage Current	I _{leakE}				1	μA
OutE1,E2 Rise Time	t ₁₁	Direct Input Mode, R _L =20Ω	30		188	ns
OutE1,E2 Fall Time	t ₁₂	Direct Input Mode, R _L =20Ω	30		188	ns
Delay from SPI Input to H-Bridge Output	t ₁₃	SPI Input Mode, R _L =20Ω		25×t _{SCK}		s

Digital Input/Output

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input	V _{in(H)}	SCK, SIN, CS, OSCIN, VD_FZ	0.54× DVDD			V
Low-level Input	V _{in(L)}	SCK,S IN, CS, OSCIN, VD_FZ			0.25× DVDD	V
RSTB Signal Pulse	t _{rst}		100			μs
Input Maximum Hysteresis Error	V _{hysin}	SCK,SIN,CS,VD_FZ		0.34		V
Image Synchronous Signal Width	VD _w		80			μs
CS Signal Wait Signal 1	t _(VD-CS)		400			ns
CS Signal Wait Signal 2	t _(CS-DT1)		5			μs

Thermal Shutdown

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Temperature for Thermal Shutdown	T _{tsd}			145		°C
Maximum Hysteresis Error for Thermal Shutdown	ΔT _{tsd}			35		°C

Power Supply Monitor Circuit

Parameter	Symbol	Condition	Min	Typ	Max	Unit
3.3V Reset	V _{rston}			2.48		V
3.3V Reset Maximum Hysteresis Error	V _{rsthys}			0.2		V
MVCCB Reset	V _{rstFZon}			2.42		V
MVCCB Reset Maximum Hysteresis Error	V _{rstFZhys}			0.21		V

FUNCTION DESCRIPTION

1. Serial Interface

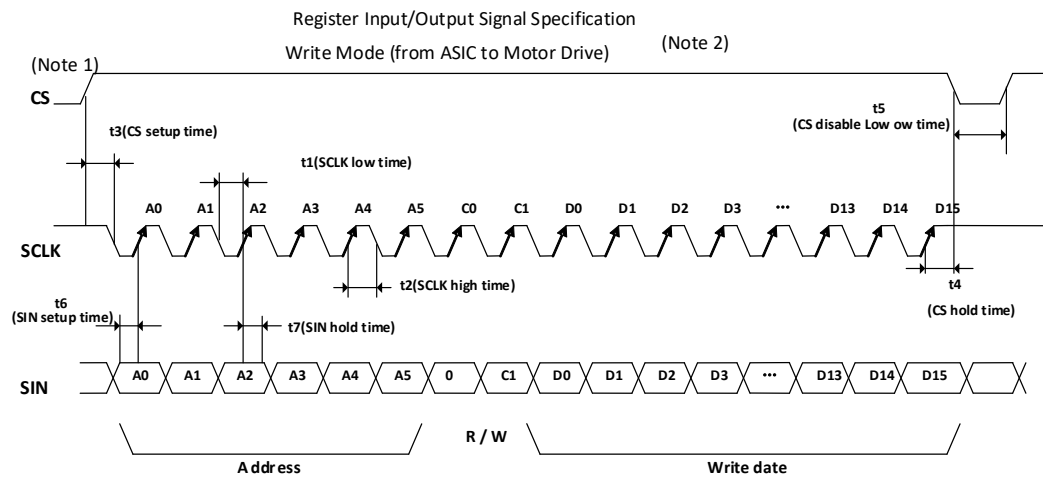


Figure 1. Data Write

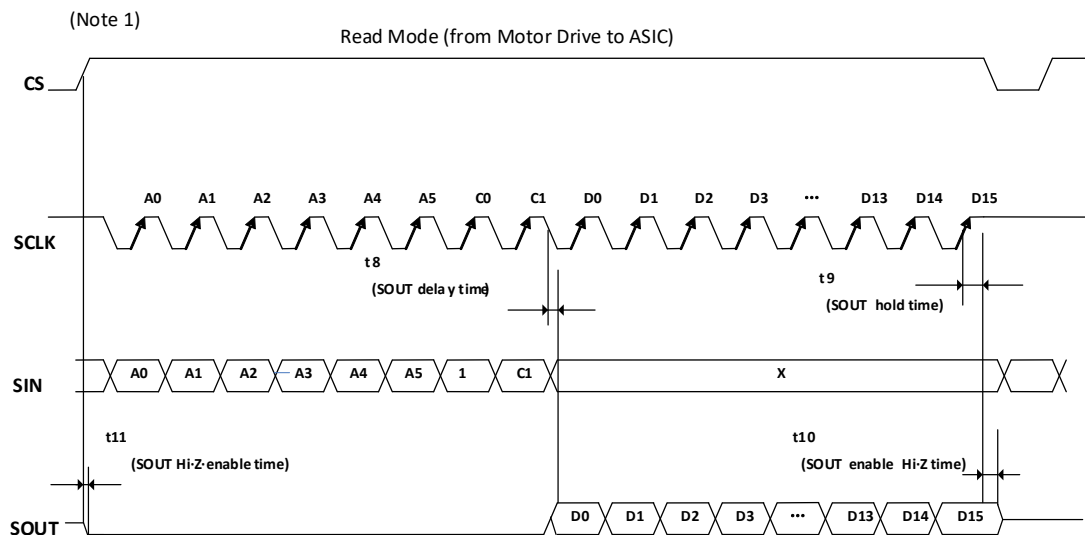


Figure 2. Data Read

Note: 1. In read/write mode, CS starts from 0 by default every cycle.

2. When in write mode, the system clock must be input from OSCIN terminal.

Electrical Parameters (Design Reference)

VDD5=MVCCB = 5V, DVDD = 3.3V.

Unless other noted, $T_A = 25^{\circ}\text{C} \pm 2^{\circ}\text{C}$. The characteristics are only design values and only for references.

1.1 Serial Port Input

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Serial Clock	Sclock				5	MHz
SCK Low Time	t1		100			ns
SCK High Time	t2		100			ns
CS Setup Time	t3		60			ns
CS Hold Time	t4		60			ns
CS Low Time	t5		100			ns
SIN Setup Time	t6		50			ns
SIN Hold Time	t7		50			ns
SOUT Delay Time	t8				200	ns
SOUT Hold Time	t9		60			ns
SOUT Enable-Hi-Z Time	t10				60	ns
SOUT Hi-Z-Enable Time	t11				60	ns
SOUT Capacitor Load	tsc				40	pF

1. The data conversion starts on the rising edge of CS and stops on the falling edge of CS.
2. The data stream unit of a conversion is 24 bits.
3. When the address and data are input from the SIN pin, the clock signal SCK remains consistent under the condition of CS=1.
4. The data is driven into IC on the rising edge of SCK signal. At the same time, when the data is output, it is read out from SOUT pin (the data is output on the rising edge of SCK).
5. SOUT outputs a high impedance state when CS=0, and when CS = 1, outputs "0" unless there is a data read.
6. The control of entire serial interface is reset when CS=0.

1.2 Data Format

0	1	2	3	4	5	6	7
A0	A1	A2	A3	A4	A5	C0	C1

8	9	10	11	12	13	14	15
D0	D1	D2	D3	D4	D5	D6	D7

16	17	18	19	20	21	22	23
D8	D9	D10	D11	D12	D13	D14	D15

C0: Register Read and Write Options: 0: Write Mode, 1: Read Mode

C1: Not Use

A5~A0: Register Address

D15~D0: Data Written to Register

1.3 Register Map

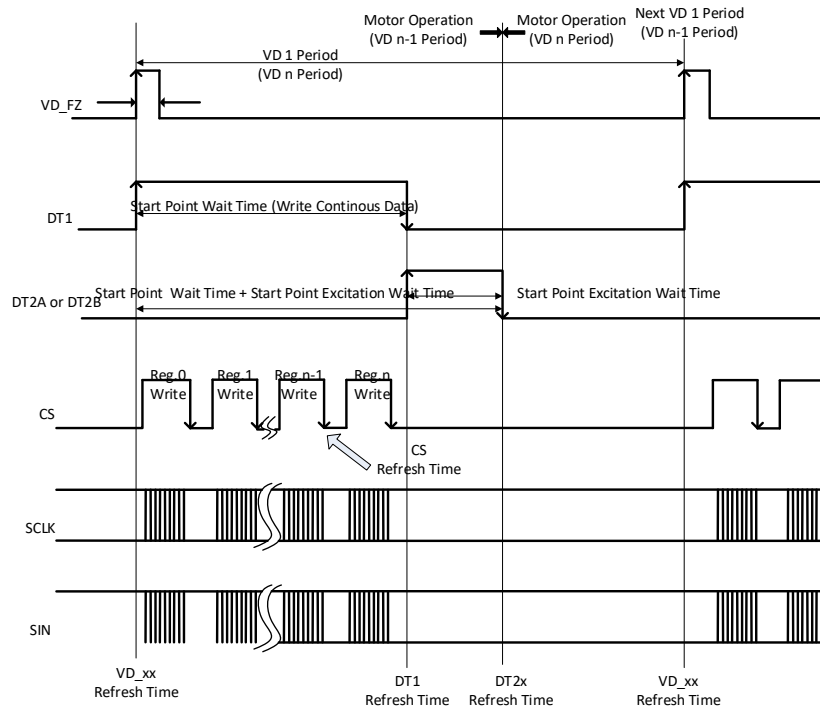
16-bit register map																
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Reserved						MODE SEL_FZ	Reserved	TEST EN1			Reserved				
20H		PWMRES [1:0]		PWMMODE[4:0]					DT1[7:0]							
21H									TEST EN2			FZTEST[4:0]				
27H			PHMODCD[5:0]						DT2B[7:0]							
28H	PPWD[7:0]								PPWC[7:0]							
29H			MICROCD [1:0]			ENDISCD	BRAKE CD	CCWCW CD	PSUMCD[7:0]							
2AH	INTCTCD[15:0]															
2CH														IN SWICH	IN1	IN2

1.4 Register List

Address	Register Name/Bit Width	Description	Page
0Bh	TESTEN1	TEST Mode Enable 1	25
	MODESEL_FZ	VD_FZ Polarity Select	15
20h	DT1[7:0]	Start Point Wait Time	19
	PWMMODE[4:0]	Microstep Output PWM Frequency	20
	PWMRES[1:0]	Microstep Output PWM Resolution	20
21h	FZTEST[4:0]	PLS1/2 Output Signal Select	25
	TESTEN2	TEST Mode Enable 2	25
27h	DT2B[7:0]	Start Point Excitation Wait Time (β Motor)	19
	PHMODCD[5:0]	Phase Correction (β Motor)	21
28h	PPWC[7:0]	Peak Pulse Width of C Channel	21
	PPWD[7:0]	Peak Pulse Width of D Channel	21
29h	PSUMCD[7:0]	Step Number of Stepper Motor (β Stepper Motor)	22
	CCWCWCD	Rotation Direction (β Motor)	22
	BRAKECD	Brake State (β Motor)	23
	ENDISCD	Enable/Disable (β Motor)	23
	MICROCD[1:0]	Sine Wave Microstep (β Motor)	23
2Ah	INTCTCD[15:0]	Microstep Cycle (β Motor)	24
2Ch	INSWICH	DC Motor Enable	
	IN1	DC Motor Input Control 1	
	IN2	DC Motor Input Control 2	

All register bit data is initialized at RSTB = 0.

1.5 Register Setup Time

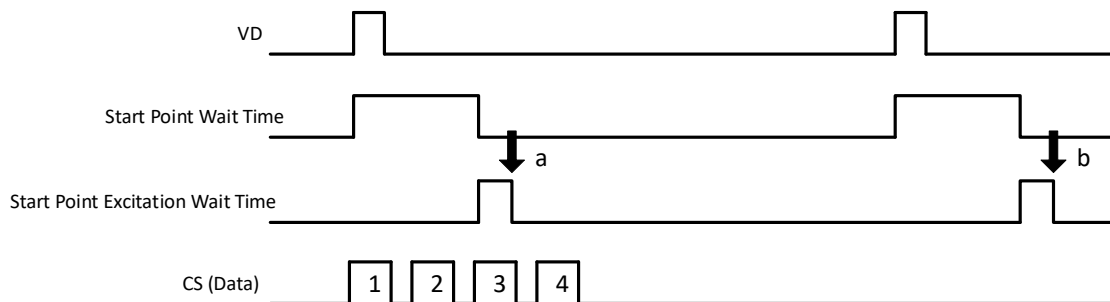


Address	Name	Setup Time
0Bh	TESTEN1	CS
	MODESEL_FZ	CS
2Ch	INSWICH	CS
	IN1	CS
	IN2	CS
20h	DT1[7:0]	VD_FZ
	PWMODE[4:0]	DT1
	PWMRES[1:0]	DT1
21h	FZTEST[4:0]	CS
	TESTEN2	CS
27h	DT2B[7:0]	DT1
	PHMODCD[5:0]	DT2B
28h	PPWC[7:0]	DT1
	PPWD[7:0]	DT1
29h	PSUMCD[7:0]	DT2B
	CCWCWCD	DT2B
	BRAKECD	DT2B
	ENDISCD	DT1 or DT2B*
	MICROCD[1:0]	DT2B
2Ah	INTCTCD[15:0]	DT2B

* 0→1: it works on DT1 ; 1→0: it works on DT2x

In principle, the setup of registers for microsteps should be completed during the time period when the start point is delayed (see figure on page 14). Data written outside the start delay can also be stored in registers. However, if the write operation is executed after the refresh time, the written register will not be valid at the scheduled time. For example, if the updated data 1~4 is written as shown in the following figure after the start point excitation delay, data 1 and 2 are immediately updated at time a, and data 3 and 4 are updated at time b. Even if the data is written continuously, the update time interval is 1 VD cycle.

For the above reasons, in order to update data timely, the establishment of the register data needs to be completed during the start point delay.



2. VD Internal Process

In this system, the reflection time and rotation time of stepper motor are respectively based on the rising edge of VD_FZ. The polarity of VD_FZ is set by the following registers.

Register Detail

MODESEL_FZ (VD_FZ Polarity Select)

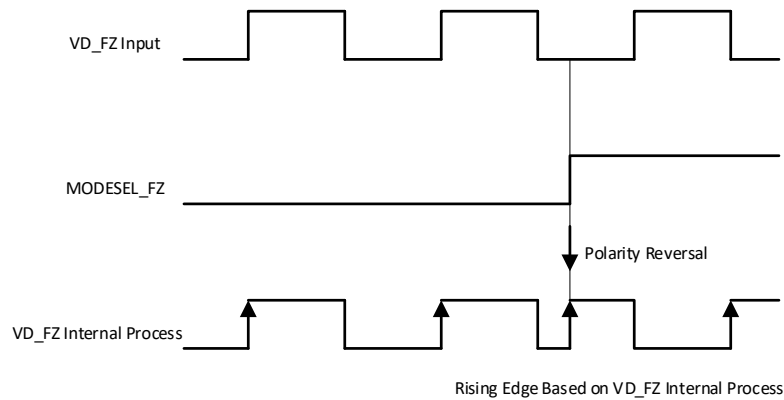
Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						MODESEL_FZ									

MODESEL_FZ sets the VD_FZ polarity.

When set to "0", the polarity is based on the rising edge of VD_FZ . When set to "1", the polarity is based on the falling edge of VD_FZ .

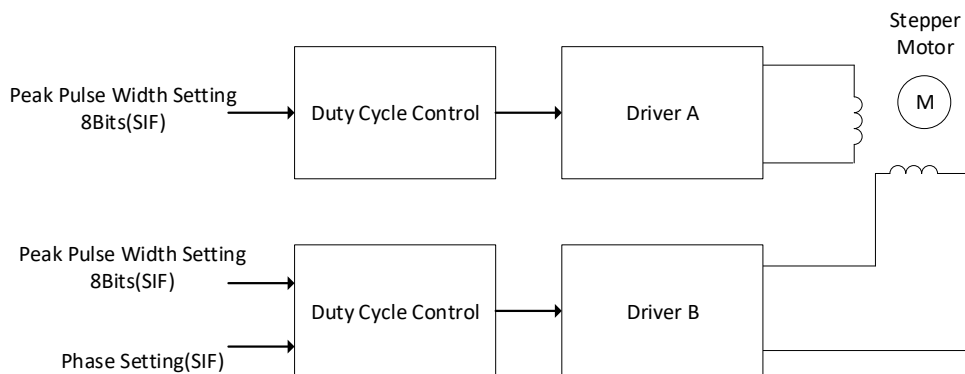
MODESEL_FZ selects the polarity of input VD_FZ. Based on MODESEL_FZ select time, The edge would be generated as shown below and is independent of VD_FZ edge.

Set Value	VD Polarity
0	Non-inverting
1	Inverting



3. Stepper Motor Microstep Drive

3.1 Block Diagram



The block for stepper motor driver used to focus and magnify. The following settings can be used to perform a series of controls. The following is the description of the motor α : driver A/B. C, D perform the same algorithm as the motor α .

Main Setting Parameters:

Phase correction: The phase difference between driver A and driver B is targeted on 90° , and can be adjusted from -22.5° to $+21.8^\circ$. —>PHMODCD[5:0]

Amplitude Setting: Set the load current of driver A/B independently —>PPWC[7:0],PPWD[7:0]

PWM Frequency: PWM frequency setting of driver output —>PWMMODE[4:0],PWMRES[1:0]

Microstep Number: Can be set to 64,128, 256 —>MICROVD[1:0]

Step Cycle: Motor Rotation Speed Setting. It is independent of microstep mode of sine wave. —>INTCTCD[15:0]

3.2 Setup Time of Related Settings

The setup time and related time are shown below.

If the related registers are updated, a setting load refresh is implemented for each VD cycle. When the same setting is executed with more than 2VD pulses, it is not necessary to write register data on each VD pulse.

DT1[7:0] (Start Point Delay, Address 20h)

Update data time setting. It must be set after the system hardware reset (Pin RSTB: Low → High), before starting excitation and driving motor (DT1 ends).

Since this setting is updated every time a VD pulse comes, it is not necessary to write during the start point delay.

PWMODE[4:0],PWMRES[1:0] (Microstep Output PWM Frequency, Address 20h)

Set PWM frequency of the microstep output. Need to be set to execute before starting excitation and driving motor (DT1 ends).

DT2B[7:0] (Start Point Excitation Delay, Address 27h)

Update data time setting. It must be set after reset (Pin RSTB: Low → High), before starting excitation and driving motor (DT1 ends).

PHMODCD[5:0] (Phase Correction, Address 27h)

By correcting the phase difference between coils A and B, the driver produces less noise. The appropriate phase correction must be based on the rotation direction and speed. This setting needs to change with the rotation direction (CCWCWAB) or the rotation speed (INTCTAB).

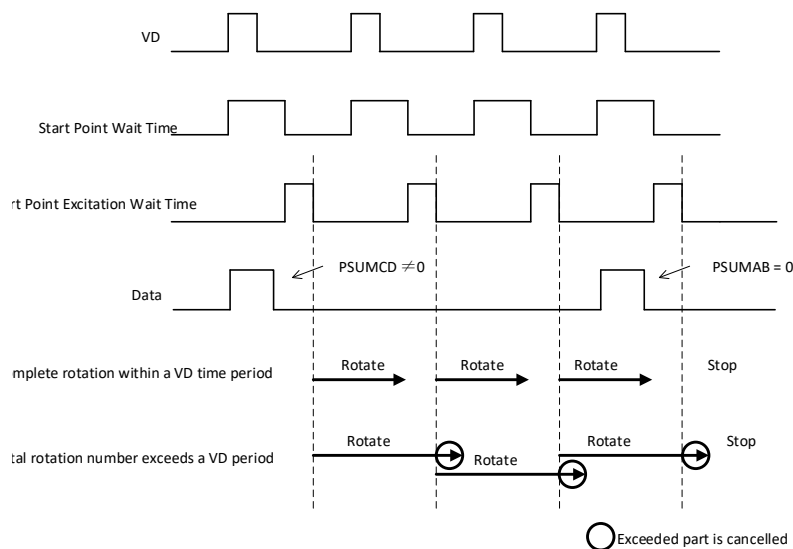
PPWC[7:0],PPWD[7:0] (Peak Pulse Width, Address 28h)

Set the PWM maximum duty cycle. Setting needs to be set before starting excitation and driving motor (DT1 ends).

PSUMCD[7:0] (Step Number of Stepper Motor, Address 29h)

The rotation number of the motor is set within 1 VD time interval.

The number of the motor rotation is set when each VD pulse is input. Therefore, setting the time to "0" can stop the motor rotation. When the total number of rotations exceeds the time of 1 VD pulse, the exceeded part will be canceled.



CCWCWCD (Rotation Direction, Address 29h)

Motor rotation direction setting. Just set it before selecting the rotation direction.

BRAKECD (Motor Brake Setting, Address 29h)

Set the current to 0 when braking. This setting is generally used to stop the motor immediately because it is difficult to obtain final position when this setting is performed.

ENDISCD (Motor Operation Enable/Disable, Address 29h)

Set the motor work enable. When set to disable, the motor pin outputs high impedance state, and should not be set to disable while the motor is rotating.

MICROCD[1:0] (Sine Wave Frequency Division, Address 29h)

Set the frequency division number of sine wave. This setting does not change the number and speed of rotation. It is set only when the rotation speed doesn't reach the demand. After reset (Pin RSTB: Low→High), setting is effective.

INTCTCD[15:0] (Pulse Period, Address 2Ah)

Pulse period setting. The rotation speed depends on this setting.

3.3 How to adjust the register value when the stepper motor is driven by microstep

In order to control lens, it is required to set the number and speed of motor rotation for each VD. The related registers are:

INTCTxx[15:0]: Set the time of each step (corresponding to the rotation speed)

PSUMxx[7:0]: Total number of rotation steps in each VD period

When the motor is continuously driven in a continuous VD period, the continuous rotation time needs to be set to adapt to the VD period.

The followings are how to calculate INTCTxx[15:0] and PSUMxx[7:0] when the motor is rotating.

- 1) Calculate INTCTxx[15:0] (determine the motor rotation speed)

$$\text{INTCTxx}[15:0] \times 768 = \text{OSCIN Frequency} / \text{Rotation Frequency}$$

- 2) PSUMxx[7:0] is calculated by INTCTxx[15:0]. Don't just only look at the value of PSUMxx[7:0].

When the following equation holds, the continuous rotation time and VD time are same, and the motor achieves uniform rotation.

$$\text{INTCTxx}[15:0] \times \text{PSUMxx}[7:0] \times 24 = \text{OSCIN Frequency} / \text{VD Frequency}$$

- 3) After the setting of PSUMxx[7:0] is completed, INTCTxx[15:0] is recalculated from above formula.

For example, OSCIN Frequency = 27 MHz, VD Frequency = 60Hz

Calculate PSUMxx[7:0] and INTCTxx[15:0] to make the motor rotate at 800pps (1-2 phase), 800pps is equal to 100Hz, so

$$\text{INTCTxx}[15:0] = 27\text{MHz} / (100\text{Hz} \times 768) = 352$$

Corresponding

$$\text{PSUMxx}[7:0] = 1 / (60\text{Hz}) \times 27\text{MHz} / (352 \times 24) = 53$$

Recalculate INTCTxx[15:0]:

$$PSUM_{xx}[7:0] = 1/(60\text{Hz}) \times 27\text{MHz} / (53 \times 24) = 354$$

If the left side of the equation in 2) is smaller than the right side, the rotation time is smaller than the VD period, which will cause discontinuous rotation. On the contrary, rotation beyond VD time period will be canceled.

3.4 Register Detail

DT1[7:0] (Start Point Wait Time)

Address			20h			Initial Value			0Ah						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DT1[7:0]															

DT1[7:0] sets the delay time of data writing to the system (start point wait time)

The motor can be activated precisely after the start point wait time is flipped from "1" to "0". The start point wait time is calculated from the rising edge of the synchronization video signal (VD_FZ).

Because the start point delay time is mainly used to wait for the serial data to be written. The register value should be set to greater than "0". If it is "0", the corresponding data cannot be updated.

Refer to page 14 for the relationship between VD_FZ and the start point wait time.

DT1	Start Point Wait
0	Prohibit
1	303.4μs
255	77.4ms
n	$n \times 8192 / 27\text{MHz}$

DT2B[7:0] (Start Point Excitation Wait Time Motor α)

Address			27h			Initial Value			03h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DT2B[7:0]															

DT2B[7:0] set the wait delay time before the motor β start to rotate.

The motor starts to rotate after the start point excitation wait time is flipped from "1" to "0". The start point excitation wait time starts to calculate at the end of start point wait time.

This signal is a separate delay for CD. The register value should be set to greater than "0". If it is "0", the corresponding data can't be updated.

Refer to page 14 for the relationship between VD_FZ and the start point excitation wait time.

DT2	Start Point Excitation Wait
0	Prohibit
1	303.4μs
255	77.4ms
n	$n \times 8192 / 27\text{MHz}$

PWMMODE[4:0] (Microstep Output PWM Frequency)

Address			20h			Initial Value			1Ch						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			PWMMODEAB[4:0]												

PWMRES[1:0] (Microstep Output PWM Resolution)

Address			20h			Initial Value			1						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	PWMRES														

PWMMODE[4:0] sets the microstep output PWM frequency by setting the frequency division of system clock OSCIN.

PWMMODE[4:0] can be set in the range of 1 to 31. The frequency of PWM wave is same when PWMMODE = 0 and PWMMODE = 1.

PWM frequency is decided by PWMRES[1:0] and PWMMODE[4:0].

The PWM frequency is calculated by the following formula

$$\text{PWM Frequency} = \text{OSCIN Frequency} / ((\text{PWMMODE} \times 2^3) \times 2^{\text{PWMRES}})$$

When OSCIN=27MHz, PWM frequency is shown in the following table (kHz)

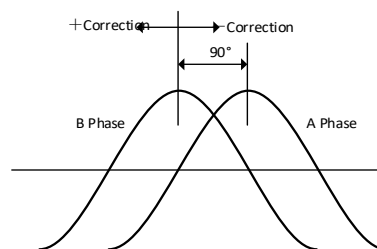
PWMMODE	PWMRES			PWMMODE	PWMRES		
	0	1	2		0	1	2
1	3375.0	1687.5	843.8	17	198.5	99.3	49.6
2	1687.5	843.8	421.9	18	187.5	93.8	46.9
3	1125.0	526.5	281.3	19	177.6	88.8	44.4
4	843.8	421.9	210.9	20	168.8	84.4	42.2
5	675.0	337.5	168.8	21	160.7	80.4	40.2
6	526.5	281.3	140.6	22	153.4	76.7	38.4
7	482.1	241.1	120.5	23	146.7	73.4	36.7
8	421.9	210.9	105.5	24	140.6	70.3	35.2
9	375.0	187.5	93.8	25	135.0	67.5	33.8
10	337.5	168.8	84.4	26	129.8	64.9	32.5
11	306.8	153.4	76.7	27	125.0	62.5	31.3
12	281.3	140.6	70.3	28	120.5	60.3	30.1
13	259.6	129.8	64.9	29	116.4	58.2	29.1
14	241.1	120.5	60.3	30	112.5	56.3	28.1
15	225.0	112.5	56.3	31	108.9	54.4	27.2
16	210.9	105.5	52.7				

PHMODCD[5:0] (Motor β Phase Correction)

Address			27h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The current phase difference in motor β is set by PHMODCD[5:0]. The default value is 90° and set 1 unit to 0.7° . Meanwhile, the data can be subject to positive and negative deviation.

PHMODCD	Phase Correction Number
000000	$\pm 0^\circ$
000001	$+0.7^\circ$
011111	$+21.80^\circ$
100000	-22.50°
111111	-0.7°
Damping Unit	$360^\circ/512 = 0.70^\circ$



The phase difference between the stepper motor coils is generally 90° . However, due to different motors or process deviations, the phase difference will also be shifted by 90° . Therefore, even if the phase difference of the drive waveform current is 90° , but the motor itself is not 90° difference, it will produce torque ripple, and the noise still exists.

The main purpose of this setting is to reduce the torque ripple caused by motor changes.

PPWC[7:0] (Peak Pulse Width for Driver C)

PPWD[7:0] (Peak Pulse Width for Driver D)

Address			28h			Initial Value			0,0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The maximum duty cycle of the PWM wave is set by PPWC[7:0] to PPWD[7:0], which determines the position of the peak output current from driver C to D.

The maximum duty cycle is calculated by the following equation:

$$\text{Driver} \times \text{Maximum Duty Cycle} = \text{PPWx} / (\text{PWMMODE} \times 8)$$

When PPWx = 0, coil current is 0.

For example, when PPWA[7:0]=200, PWMMODE[4:0]=28, maximum duty cycle is:

$$200 / (28 \times 8) = 0.89$$

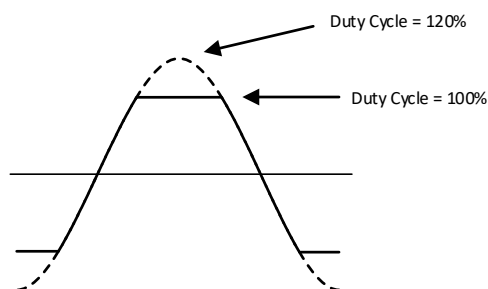
Depending on the values of PWMMODE and PPWx, the maximum duty cycle may exceed 100%.

Of course, the duty cycle cannot exceed 100% in fact and the peak point of sine wave will be truncated as shown in the following figure.

For example, when PWMMODE = 10, PPWx = 96,

$$\text{Maximum Duty Cycle} = 96 / (10 \times 8) = 120\%$$

The waveform of the target current is shown as follows:



PSUMCD[7:0] (Step Number of Motor β)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PSUMCD[7:0]															

PSUMCD[7:0] sets the total step number of the motor β .

If want to stop the motor, set PSUMxx[7:0]=0.

Register Value	Total Step Number		
	64 Microstep	128 Microstep	256 Microstep
0	0	0	0
1	2	4	8
255	510	1020	2040
n	2n	4n	8n

As long as the maximum duty cycle of PWM wave is not set as "0", when PSUMxx[7:0]=0, the motor can keep in the release state.

An example to know the meaning of setting :

When PSUMCD[7:0]=8 is set, run 16 steps in 64 microstep mode, i.e. $16/64=1/4$ sine cycle. Similarly, in 128 and 256 microstep modes, it is also a quarter of the period of sine wave.

CCWCWCD (Rotation Direction of Motor β)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							CCWCWCD								

CCWCWCD sets the rotation direction of the motor β .

Direction Definition:

Set Value	Motor Rotation Direction
0	Forward
1	Reverse

BRAKECD (Brake State of Motor β)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						BRAKECD									

BRAKECD sets the brake mode of the motor β .

Set Value	Motor Brake
0	Normal State
1	Brake State

In brake state, the two high-side PMOS FETs of H-bridge are all turned on. The brake mode cannot be used in normal operation and can only be used during emergency shutdown. It is recommended to use in abnormal state.

ENDISCD (Motor β Enable/Disable)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					ENDISCD										

ENDISCD sets the output control of the motor β .

When $ENDIS_{xx} = 0$, motor outputs high impedance state. However, internal excitation position counter still keeps counting at $ENDIS_{xx}=0$. Therefore, when you want to stop the motor in normal state, set $PSUM_{xx}[7:0] = 0$ instead of $ENDIS_{xx} = 0$.

Set Value	Motor Output State
0	Output Off (High-impedance State)
1	Output On

MICROCD[1:0] (Sine Wave Frequency Division of Motor β)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		MICROCD[1:0]													

MICROCD sets the frequency division of sine wave for motor β .

The 64 division waveform is shown on page 24.

MICROCD	Frequency Division
00	256
01	256
10	128
11	64

INTCTCD[15:0] (Step Cycle of Motor β)

Address			2Ah			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INTCTCD[15:0]															

INTCTCD[15:0] sets a microstep cycle of the motor β .

Register Value	Total Step Number		
	64 Microstep	128 Microstep	256 Microstep
0	0	0	0
1	444ns	222ns	111ns
Max	29.1ms	14.6ms	7.3ms
n	12n/27MHz	6n/27MHz	3n/27MHz

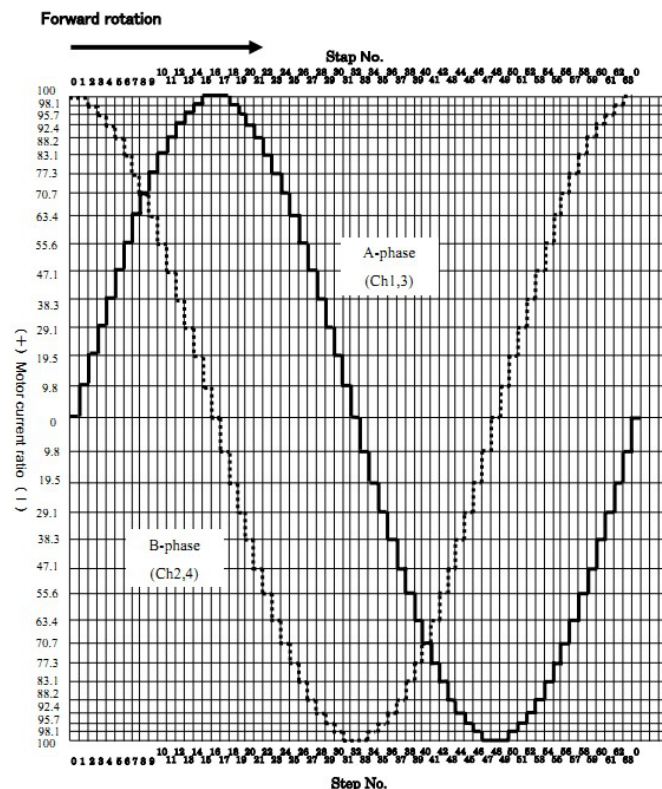
When INTCTCD[15:0]=0, as long as PWM maximum duty cycle is not 0, the motor will remain in release state.

For example: when INTCTCD[15:0]=400, step cycle in 64 microstep:

$$12 \times 400 / 27 \text{MHz} = 0.178 \text{ms}$$

Therefore, the period of each sine wave is 11.4ms (87.9Hz). Similarly, in 128 microstep or 256 microstep, it is also 11.4ms.

Stepper Motor Drive (64 Microstep Current Curve)



4. Test Signal

FZTEST[4:0] (Test Signal Output Setting)

Address			21h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												FZTEST[4:0]			

TESTEN1 (Test Setting 1)

Address			0Bh			Initial Value			0			TESTEN2			
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TESTEN1							

TESTEN2 (Test Setting 2)

Address			21h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TESTEN2							

FZTEST[4:0] selects the test signals output by PLS1 and PLS2.

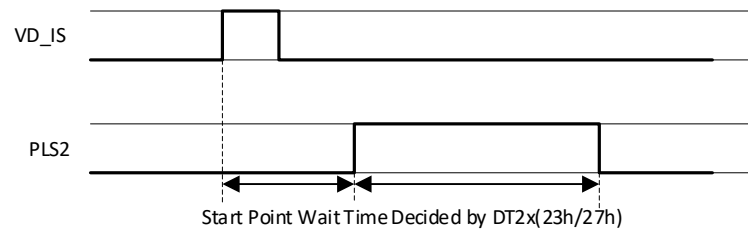
TESTEN1 and TESTEN2 need to be set to "1" to allow the test signal output.

The following table is the output setting signal.

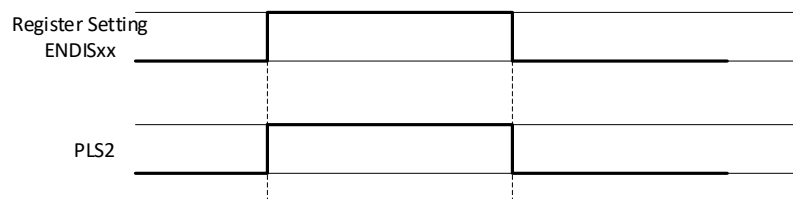
Setting	A Cycle	Description
	PLS2	
1	0	H-Bridge Output for Start Point Wait Time
2	Start Point Excitation Wait Time B	H-Bridge Output for Start Point Excitation Wait Time
3	ENDISCD	ENDISxx Setting
4	CCWCWCD	CCWCWxx Setting
5	Monitor Output Pulse B	“H”/“L” change in 64 microstep when motor is rotating
6	0	PWM Period Signal of Motor Output
7	Complete Pulse Output for Driver B	H-Bridge Output when Motor Rotating
15	“H”Bridge NMOS1 C	Monitor Driver C
16	“H”Bridge NMOS2 C	
17	“H”Bridge NMOS1 D	Monitor Driver D
18	“H”Bridge NMOS2 D	

The relevant waveforms are described as follows:

Start Point Excitation Wait Time



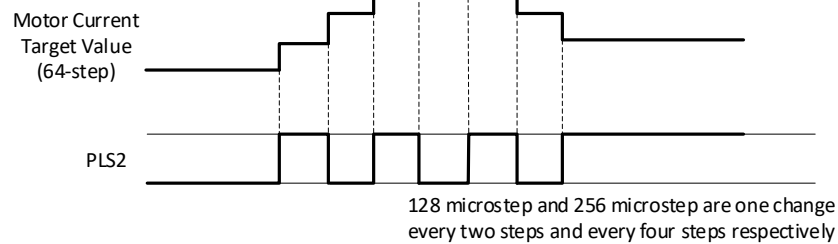
ENDISxx



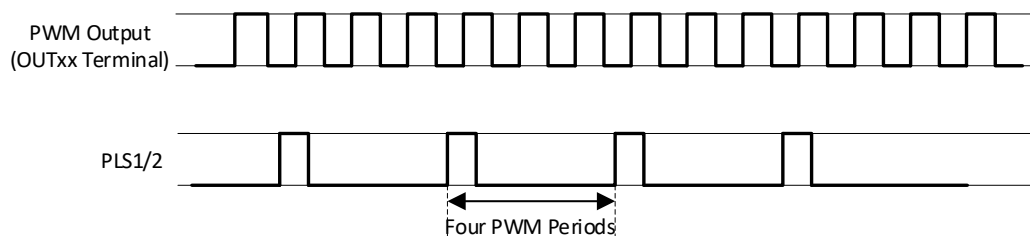
CCWCWxx



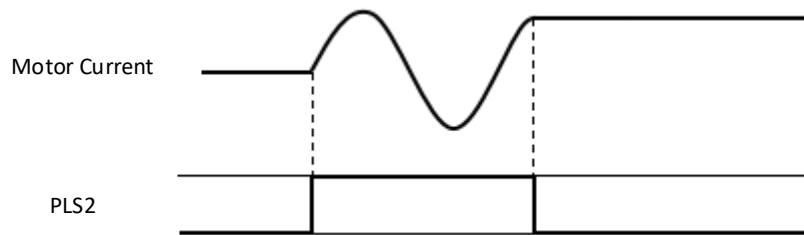
Pulse Output Monitoring



PWM Circle Monitoring

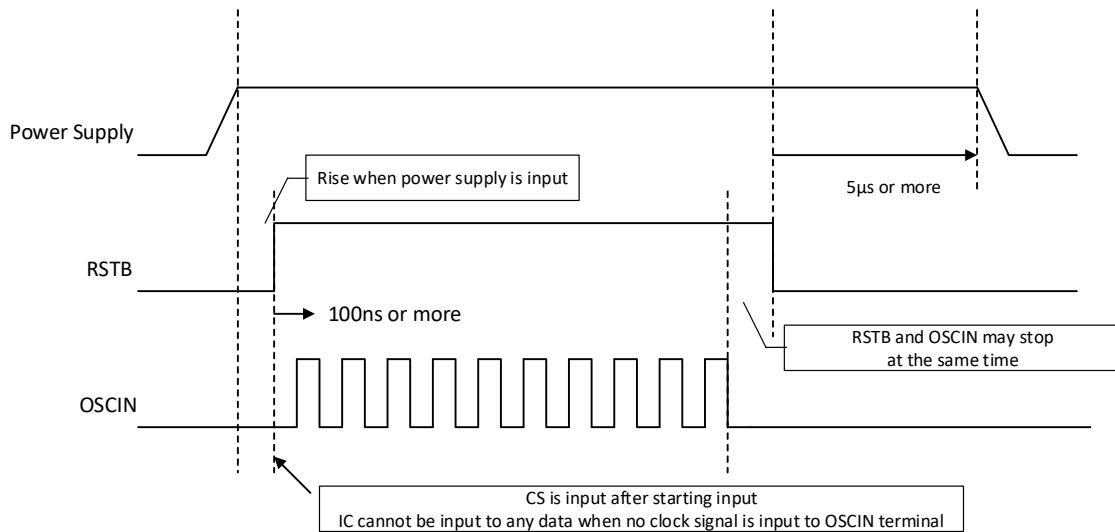


Complete Pulse Output



(1) Start and Finish Timing

The start and finish timing of power signal, RSTB and OSCIN are shown in the following figure.



(2) Input Capacitance of Input Pin

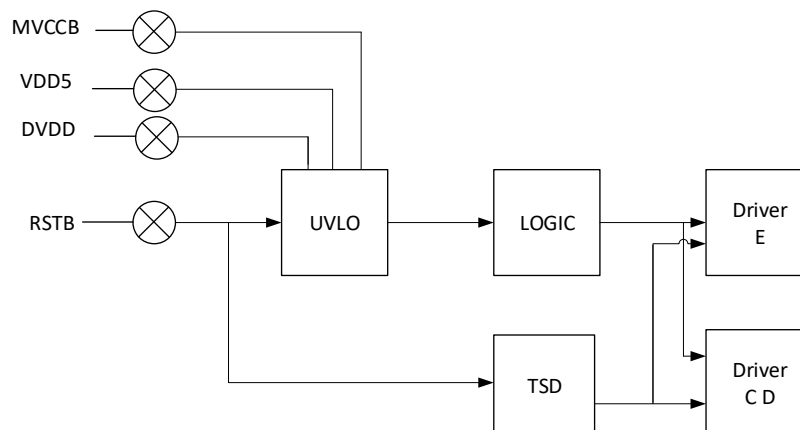
The capacitance of input pin is 10pF or less.

(3) OSCIN, VD Signal Time

Once VD signal (VD_FZ) is synchronized with OSCIN, the VD and OSCIN signals have no constraint on input time.

5. Reset/Protection Circuit

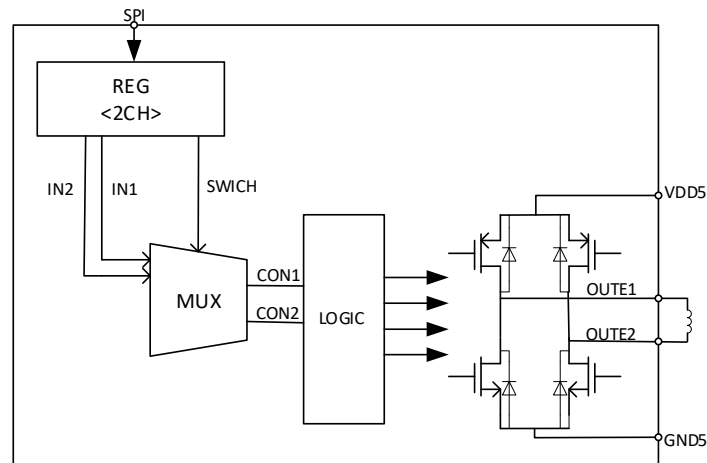
The following figure shows the relationship between RSTB, UVLO, TSD and other circuits.



The corresponding specifications are shown in the following table.

	Setting	Stepper Driver	DC Driver
RSTB	Disable	Logic Reset->Output Shutdown	
Thermal Shutdown (TSD)	×	Output Shutdown	
Undervoltage Lockout (UVLO)	×	Logic Reset->Output Shutdown	

6. DC Driver E Circuit



DC motor (used in IR-CUT in camera) driver adopts PWM control method. SWICH register in REG<2CH> bit2 is '0' by default at power-up. It must be set to '1' and SPI input is valid.

SWICH Register: Register REG_2CH<2> bit2, Power-up Default '0'. It is set to '1' when serial input.

IN1 Register: Register REG_2CH<1> bit1, Power-up Default '0'

IN2 Register: Register REG_2CH<0> bit0, Power-up Default '0'

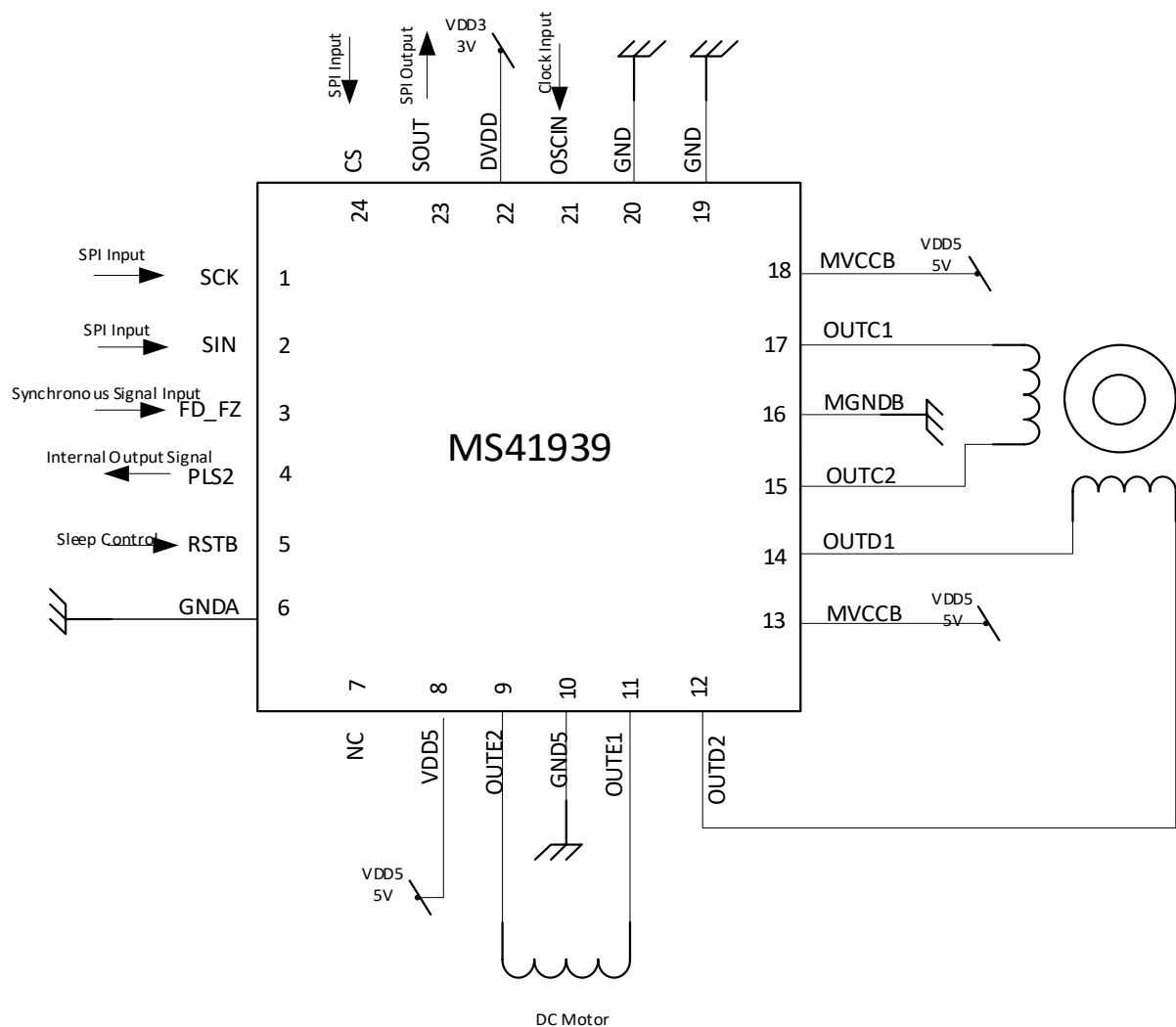
Truth table of output is as follows:

2CH Register Input	Register Value			Output		
	SWICH	IN1	IN2	OUTE1	OUTE2	Motor State
0004h	1	0	0	Z	Z	Coast
0005h	1	0	1	L	H	Reverse
0006h	1	1	0	H	L	Forward
0007h	1	1	1	L	L	Brake
Other	0	x	x	z	z	Coast

Delay Time of DC Motor in SPI Mode

22 data and 3 control bits are written every writing in SPI mode. The transmission delay is about $t_{\text{scK}} \times 25$ from writing register 2CH to actual work of control time. If the serial clock of writing data is 0.5MHz, the delay time is $25 \times 1 / 0.5\text{M} = 50\mu\text{s}$. And the maximum output frequency of H-bridge is 10kHz.

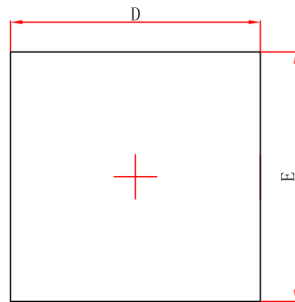
TYPICAL APPLICATION DIAGRAM



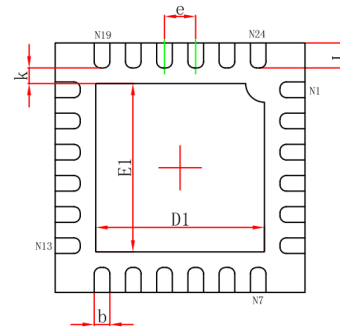
1. The MS41939 has back thermal pad and it must be grounded in large power applications.
2. OSCIN pin (PIN21) can be provided by active crystal oscillator and can be connected to output terminal of passive crystal oscillator for other chips in system such as MCU. Or it can be connected to clock output terminal for other chips.

PACKAGE OUTLINE DIMENSIONS

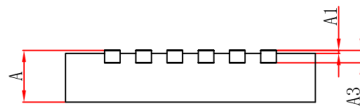
QFN24



Top View



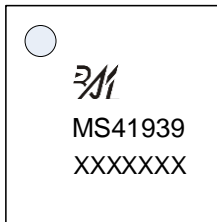
Bottom View



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
k	0.200MIN		0.008MIN	
b	0.180	0.300	0.007	0.012
e	0.500TYP		0.020TYP	
L	0.300	0.500	0.012	0.020

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: MS41939

Product Code: XXXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS41939	QFN24	4000	1	4000	8	32000

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**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



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